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# MS-7970

ATX  
Ver:  
1.1

<http://vlab.su/>

## Intel -Skylake platform Z170

### CPU:

Skylake-S

### Onboard Chip:

HD Audio Codec:ALC892

LAN:RTL 8111H

SIO:Nuvoton 6793D

Flash ROM: SPI 64MB /128MB(For  
H170/B150)

### Main

### Memory:

DDRIV (800/1066/1333/1600/2133MHz) \* 4 (Dual  
Channel)

### ACPI:

NIKO/UPi

### Expansion

### Slots:

PCI Express (X16) Slot \*1  
PCI Express (X4) Slot \*1  
PCI Express (X1 ) Slot \*3  
PCI Slot \*3  
M2 \*1

### System Chipset:

Z170 TOMAHAWK  
B150 TOMAHAWK  
Z170A G43

### PWM:

IMVP8 -ISL95858

### Other:

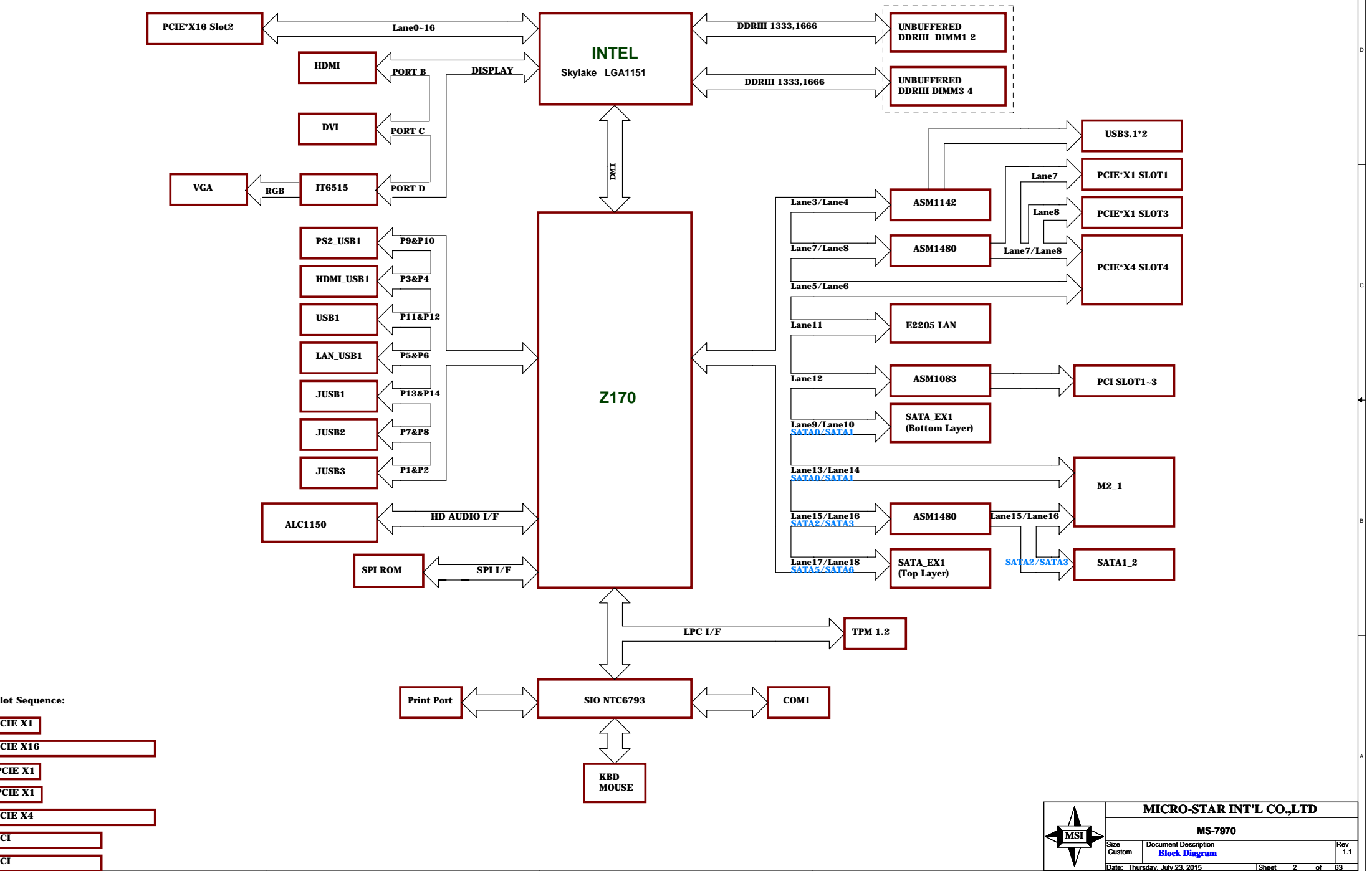
SATA3.0 x6 (PCH)  
REAR USB2.0 \*2  
FRONT USB2.0 \*4  
FRONTUSB3.0 \*4  
REAR USB3.0 \*2  
REAR USB3.1 \*2



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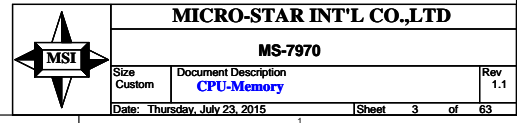


MS-7978 Block Diagram

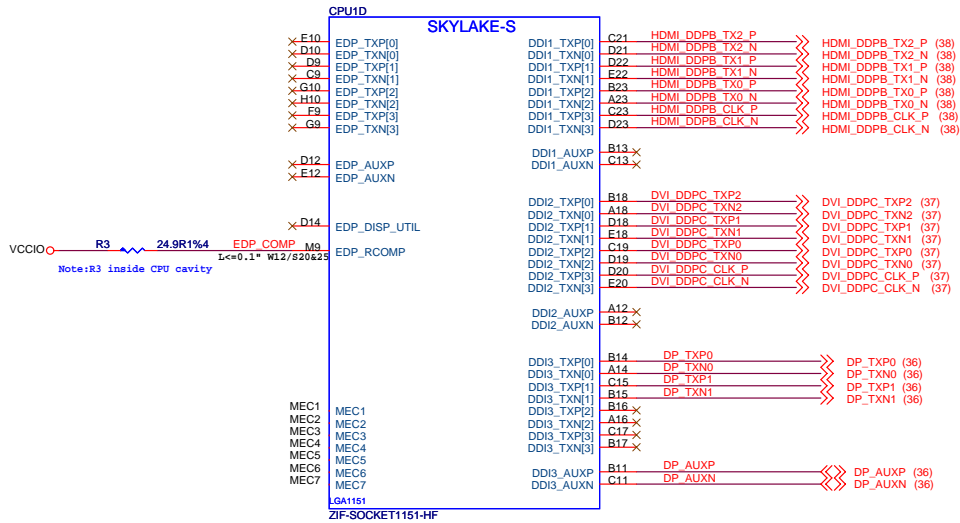
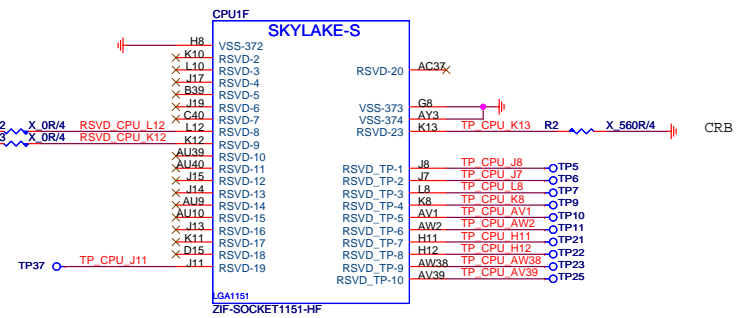
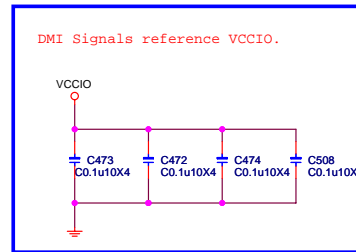
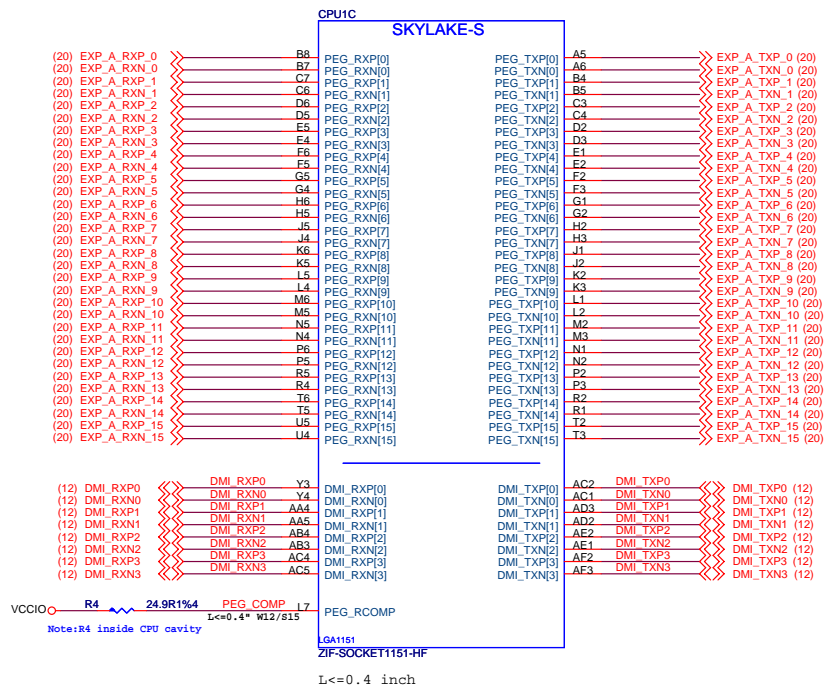


- Slot Sequence:
- PCIE X1
  - PCIE X16
  - PCIE X1
  - PCIE X1
  - PCIE X4
  - PCI
  - PCI







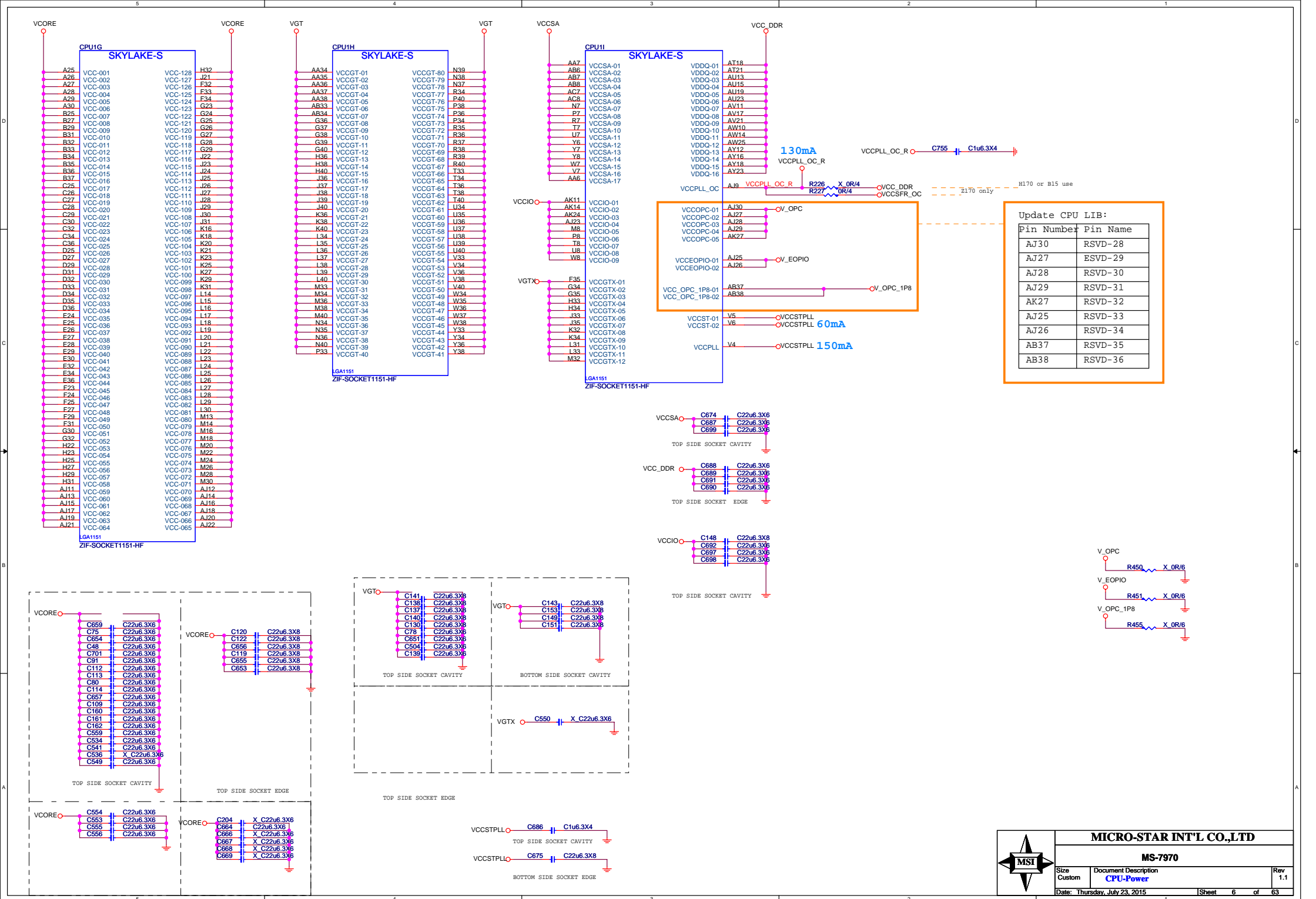


CPU Socket MEC5 Hole top layer add Soldermask,bot layer not add Soldermask.  
 1.MEC5 connect to GND.  
 2.Add CPU1L.  
 3.Footprint change to ZIF SOCK1151\_TEST\_7978.

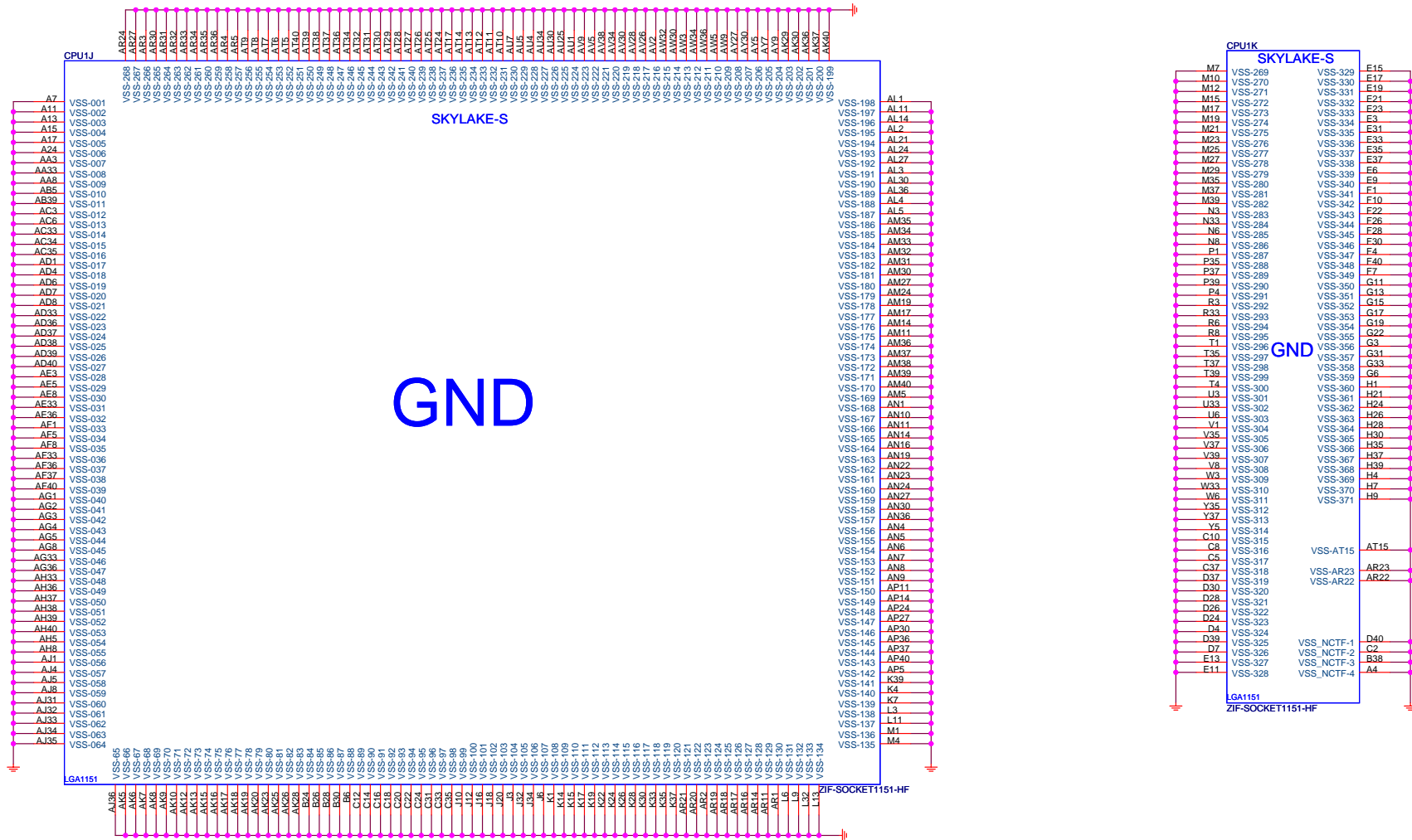




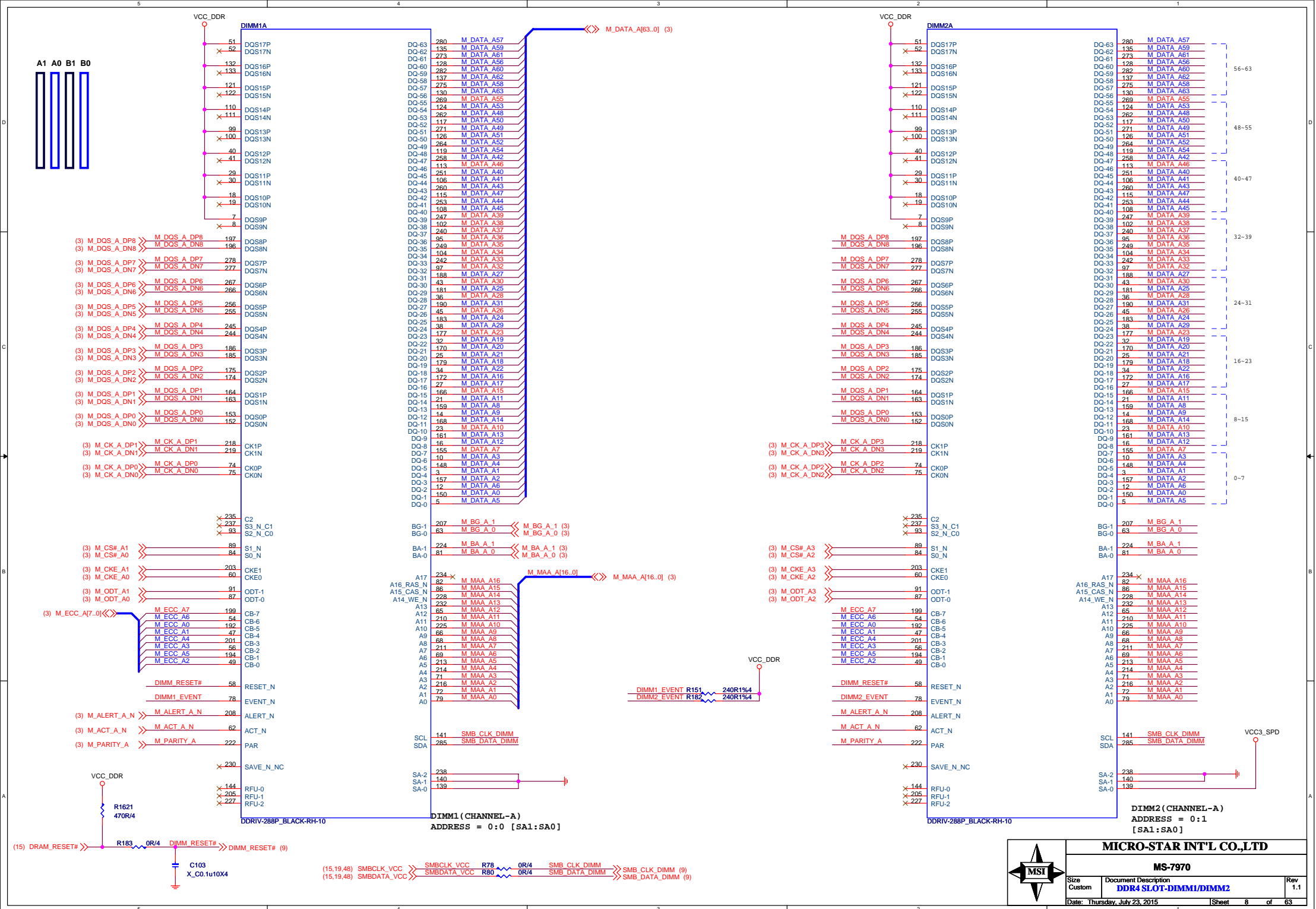








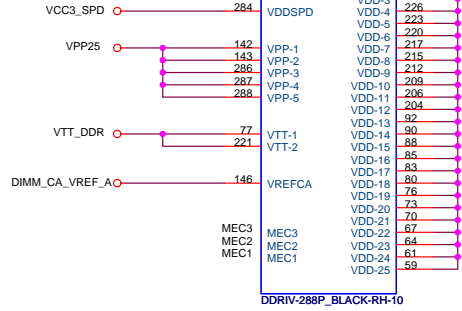
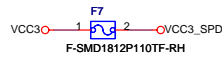




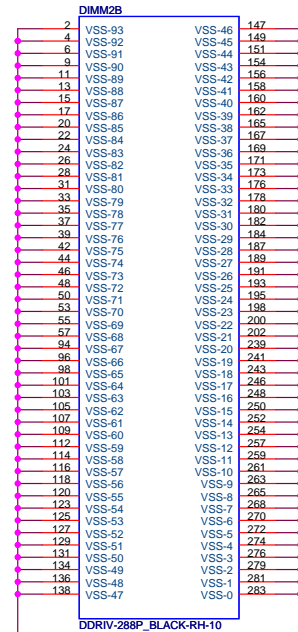
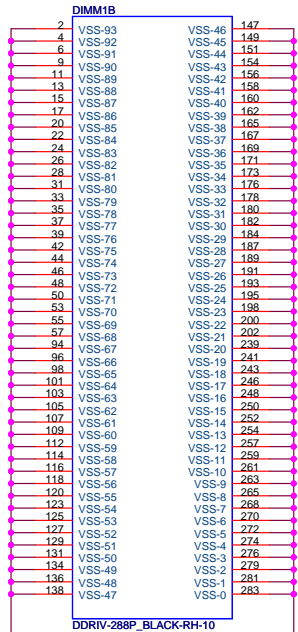
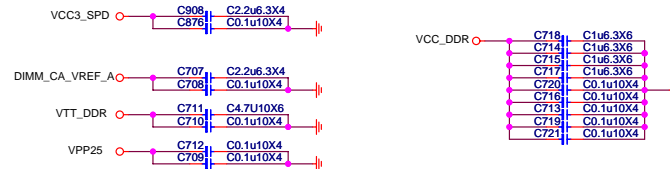
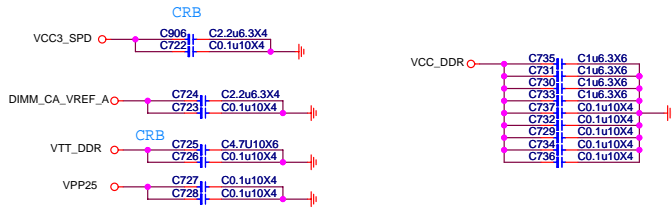
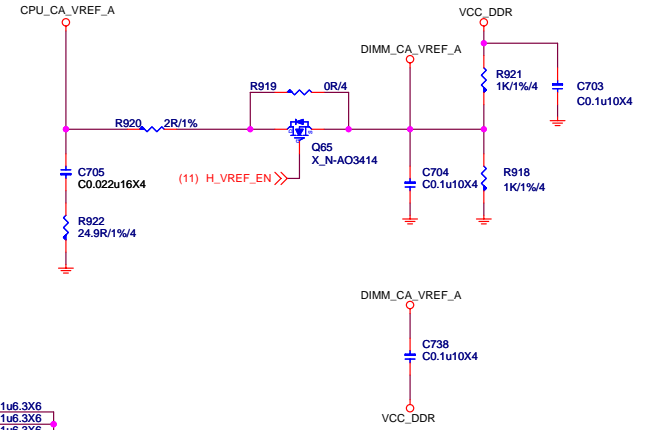
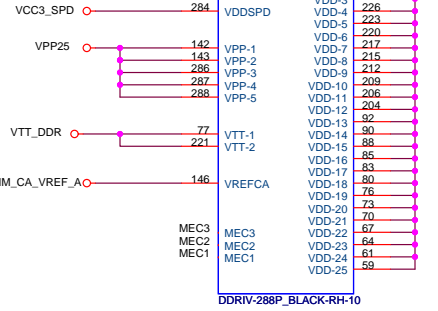
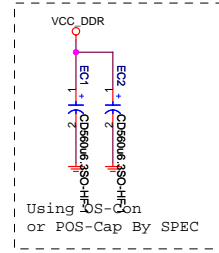




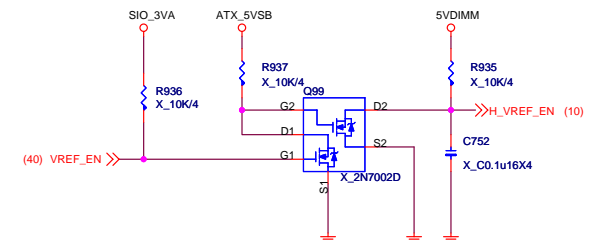
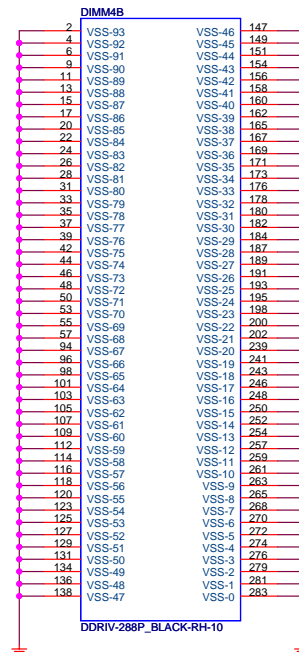
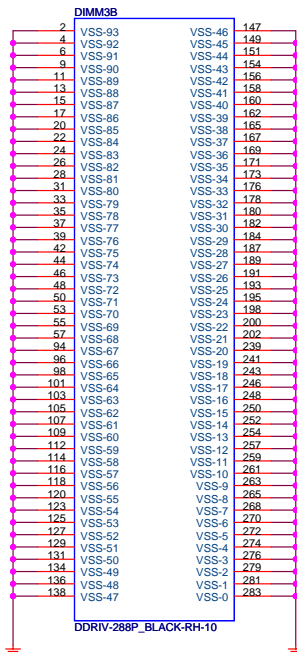
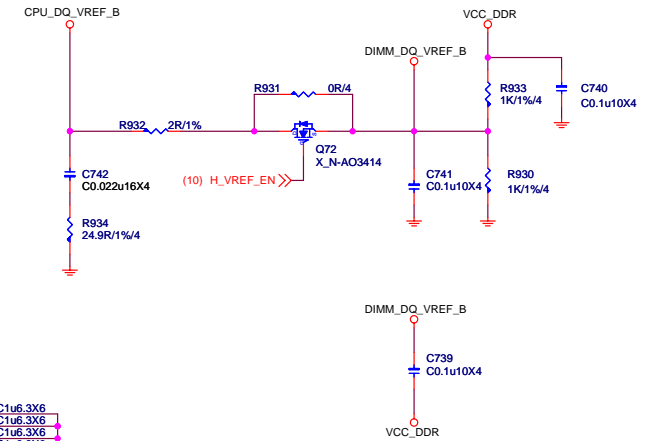
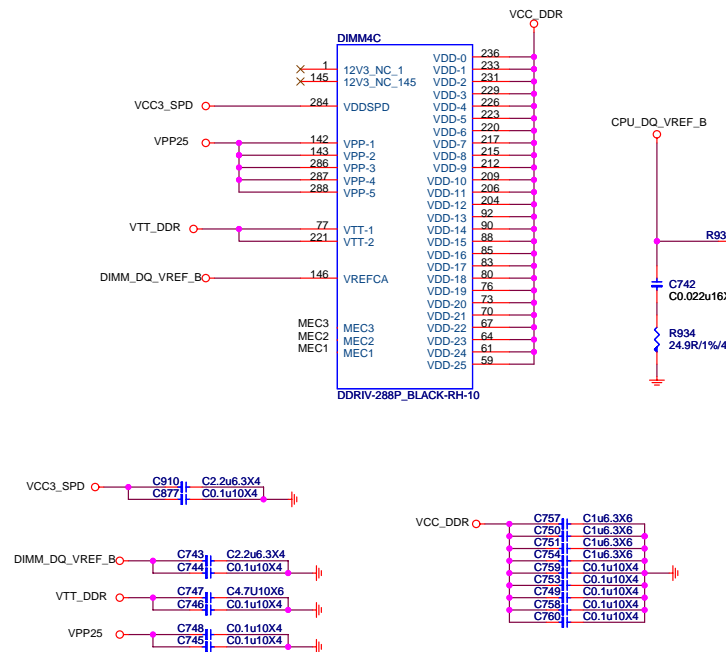
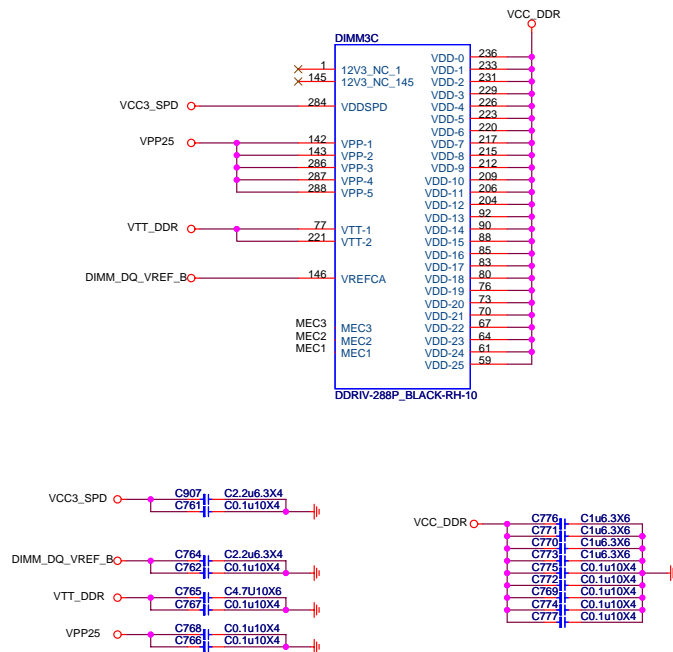




DIMM SLOT PN BY SPEC





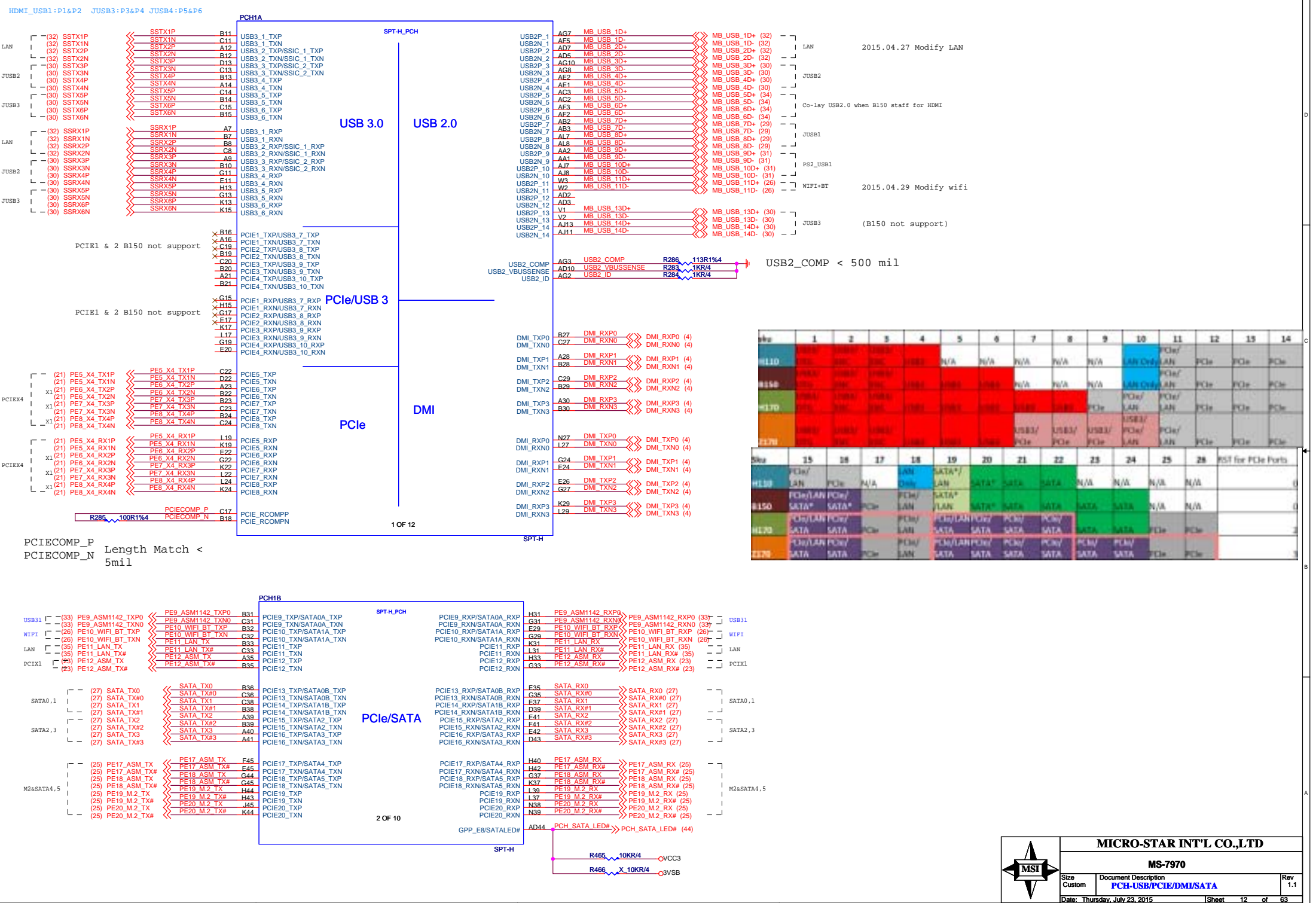


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**MS-7970**

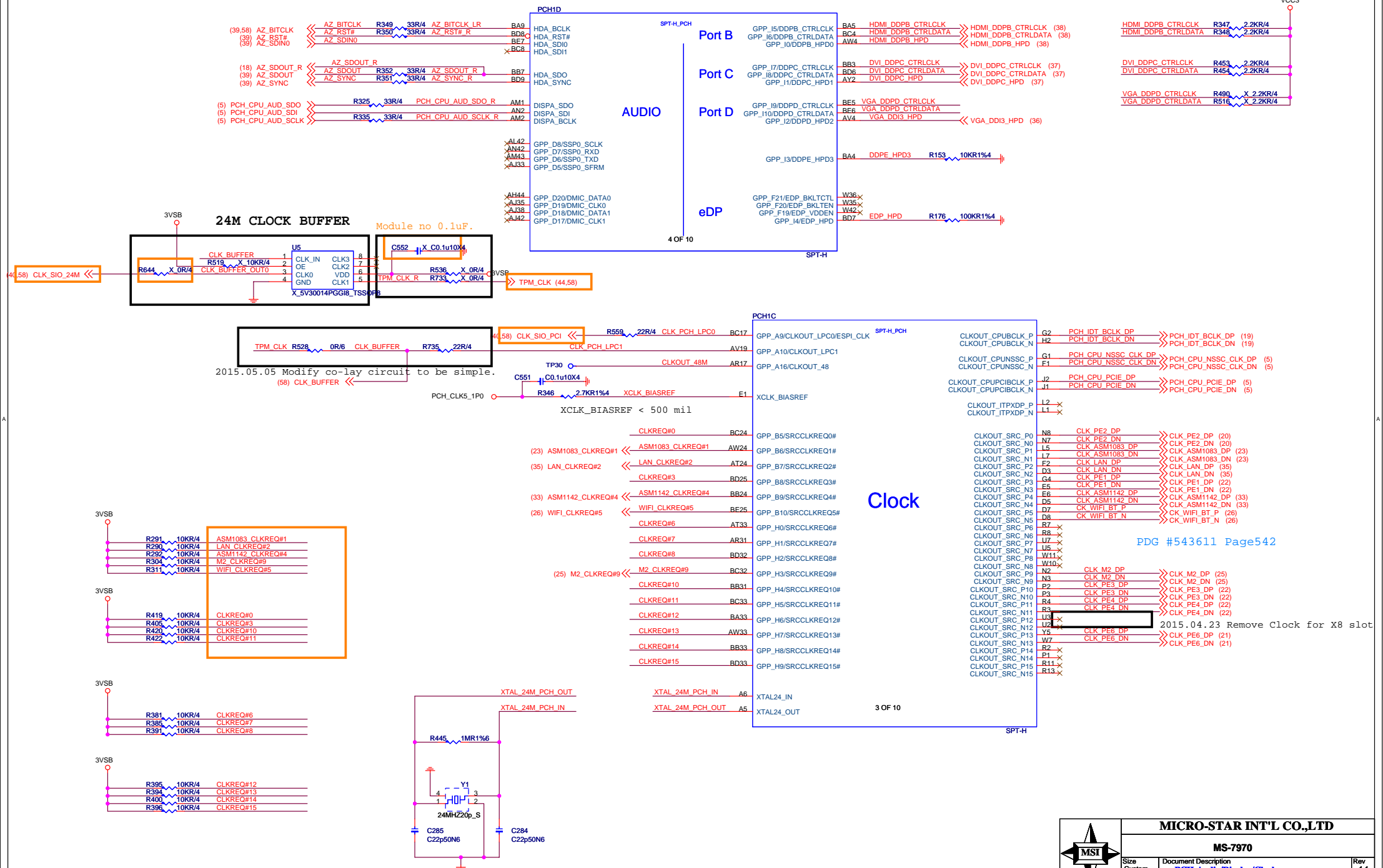
Size Custom	Document Description <b>DDR4-POWER/GND-2</b>	Rev 1.1
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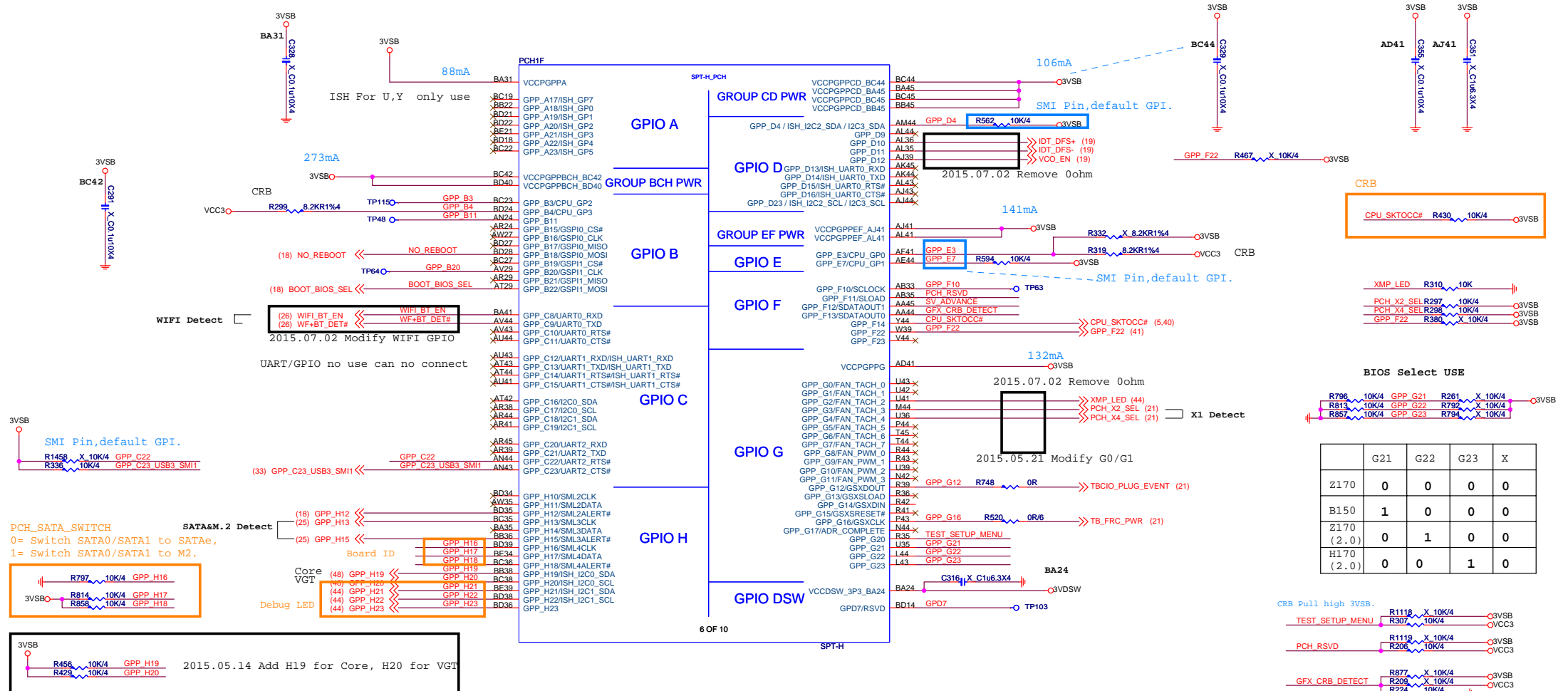




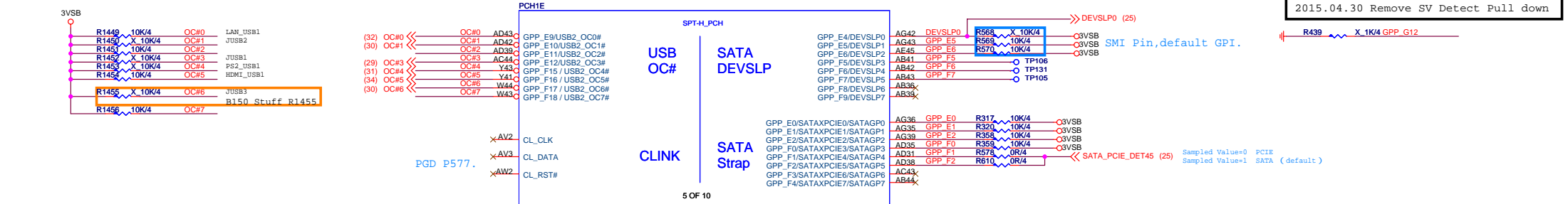
GPP\_I[3:0] with SMI/NMI







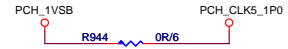
	G21	G22	G23	X
Z170	0	0	0	0
B150	1	0	0	0
Z170 (2.0)	0	1	0	0
H170 (2.0)	0	0	1	0



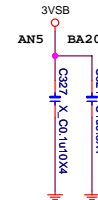
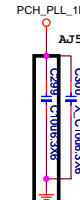
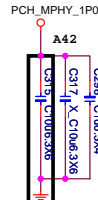
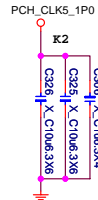
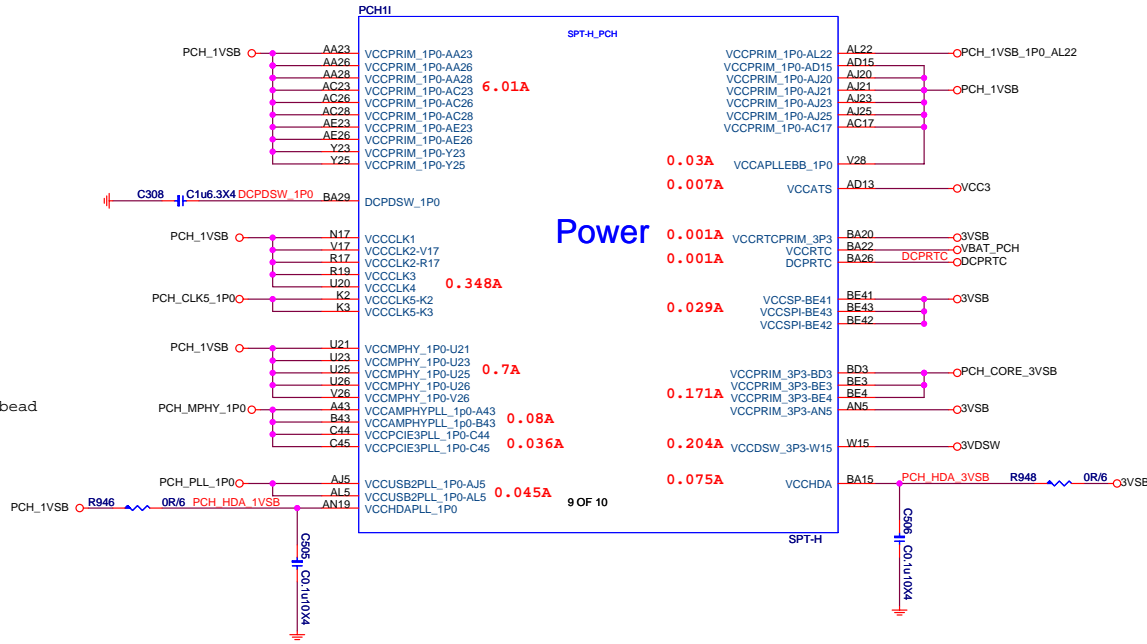
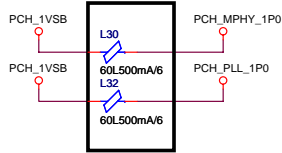




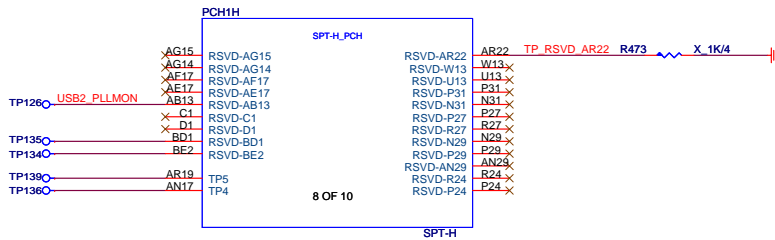
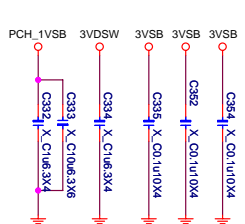




2015.05.18 Modify from 00hm to bead



BOT



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GND

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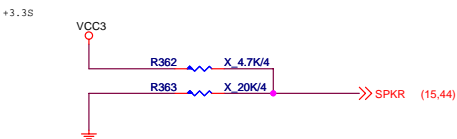
MICRO-STAR INT'L CO.,LTD

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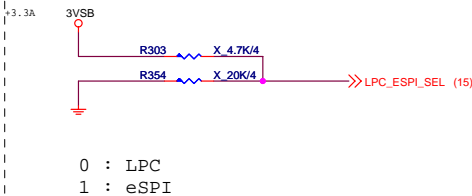


TOP Swap



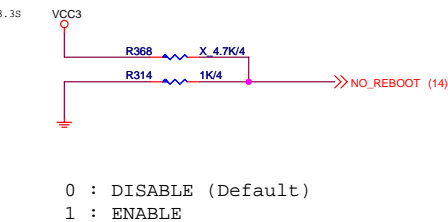
Internal pull-down is disabled after PLTRST#

LPC eSPI Mode



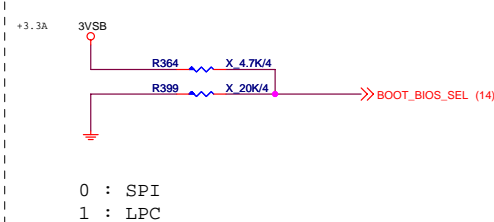
Internal pull-down is disabled after RSMRST

No Reboot



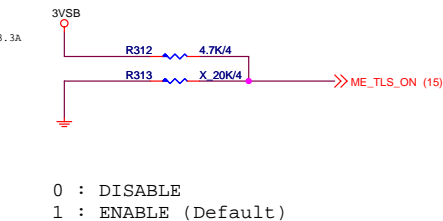
Internal pull-down is disabled after PLTRST#

Boot BIOS



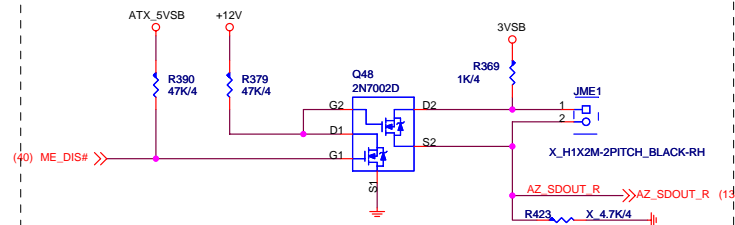
Internal pull-down is disabled after PLTRST

AMT and SBA with confidentiality

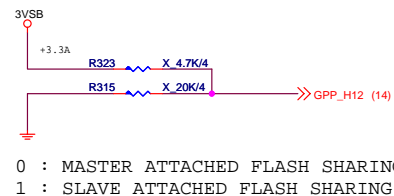


Internal pull-down is disabled after RSMRST

HDA\_SDO



ESPI FLASH SHARING MODE

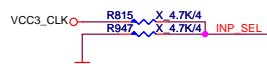
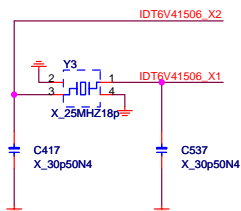


Internal pull-down is disabled after RSMRST

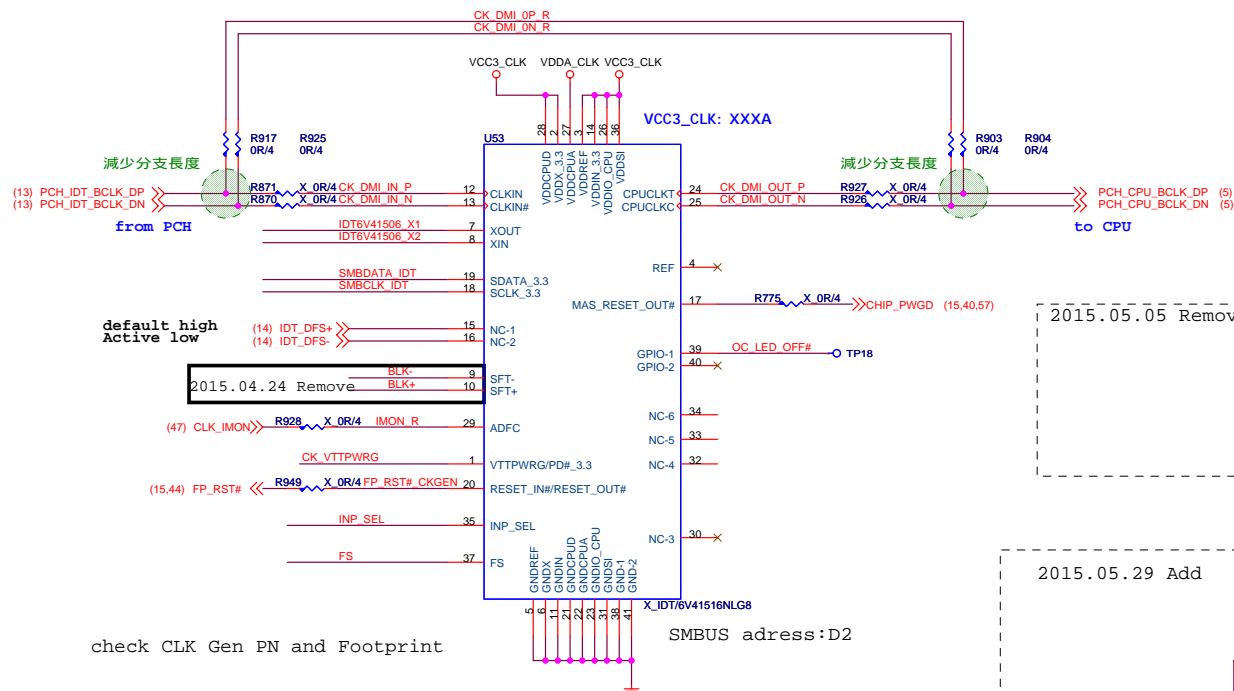


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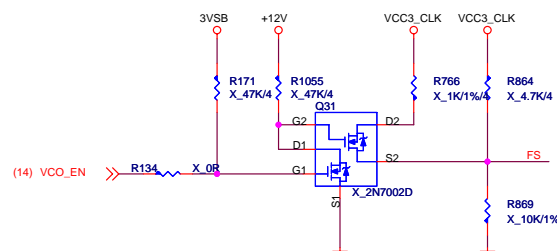
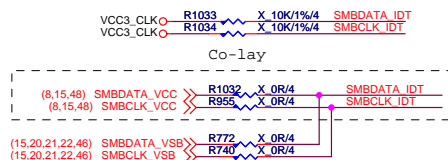
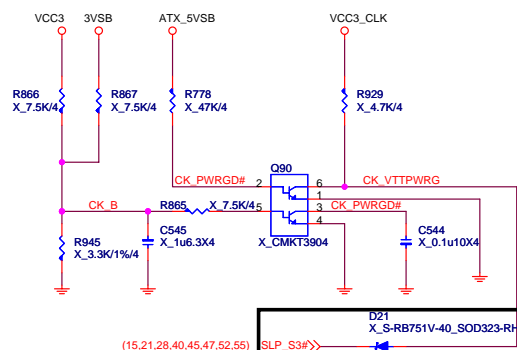
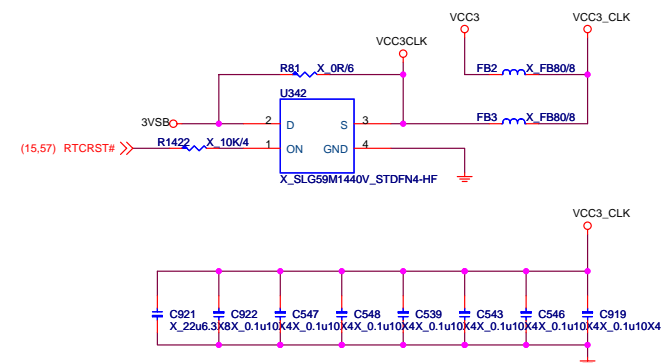
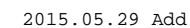
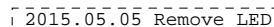




INP_SEL	
0	25MHz crystal input
1	100MHz differential input



check CLK Gen PN and Footprint



FS	VCO Frequency
0	VCO 400MHz(OC)
1	VCO 1200MHz(default)



**MICRO-STAR INT'L CO.,LTD**

**MS-7970**

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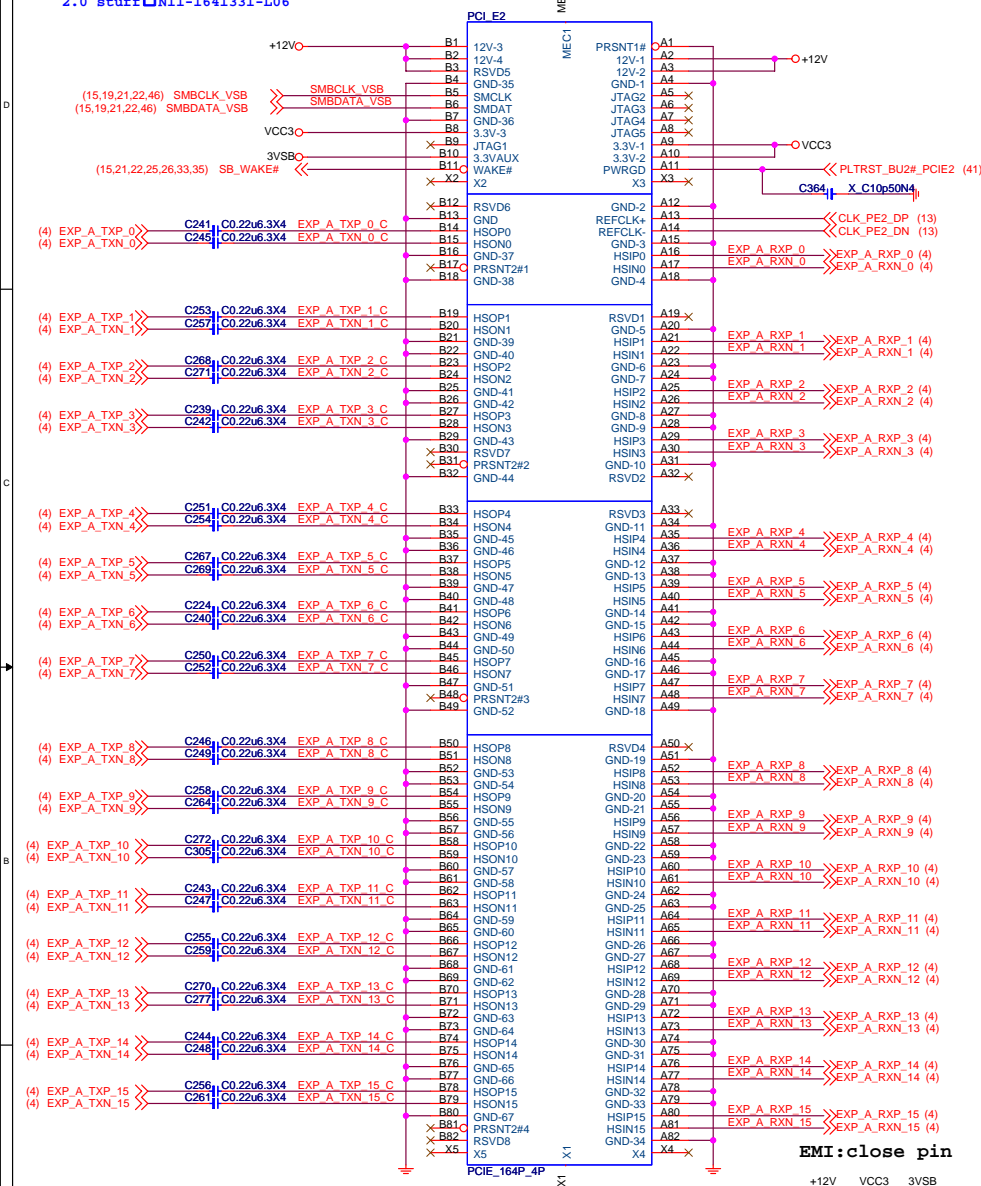


# PCI Express X16 Slot

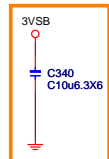
footprint UN1-7968002  
1.0 stuff UN11-1641221-L06  
2.0 stuff UN11-1641331-L06

support max speed GEN3 Black

2015.04.23 Remove switch

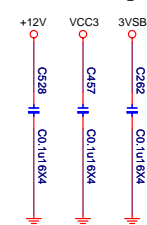


Close to slot



2015.05.04 Add for improve 5VDUAL Drop issue.

EMI:close pin



2015.04.23 Remove



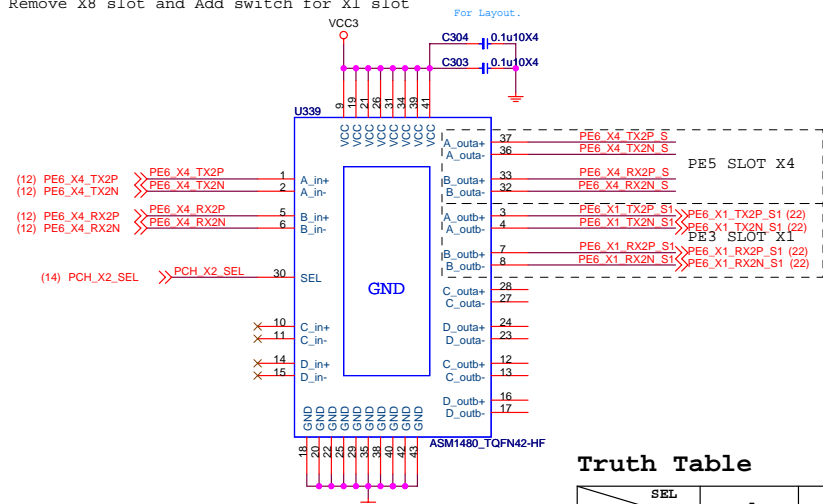
SEL	MODE_1	MODE_0
8X/8X	1	1
16X	1	0
8X/8X	0	1
16X	0	0



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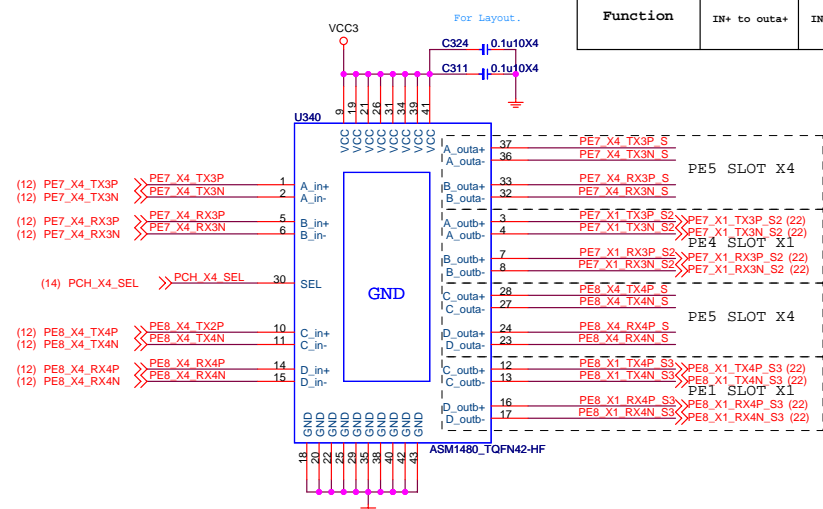


2015.04.28 Remove X8 slot and Add switch for X1 slot

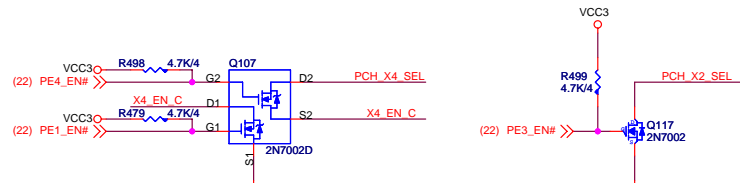


### Truth Table

SEL Function	L	H
Function	IN+ to outa+	IN+ to outh+






2015.05.22 Modify X1 detect circuit



GPP_G3	LOW(I)	HIGH(I)	LOW(I)
GPP_G4	LOW(I)	HIGH(O)	HIGH(I)
	X4/X0/X0/X0	X1/X1/X1/X1	X2/X0/X1/X1

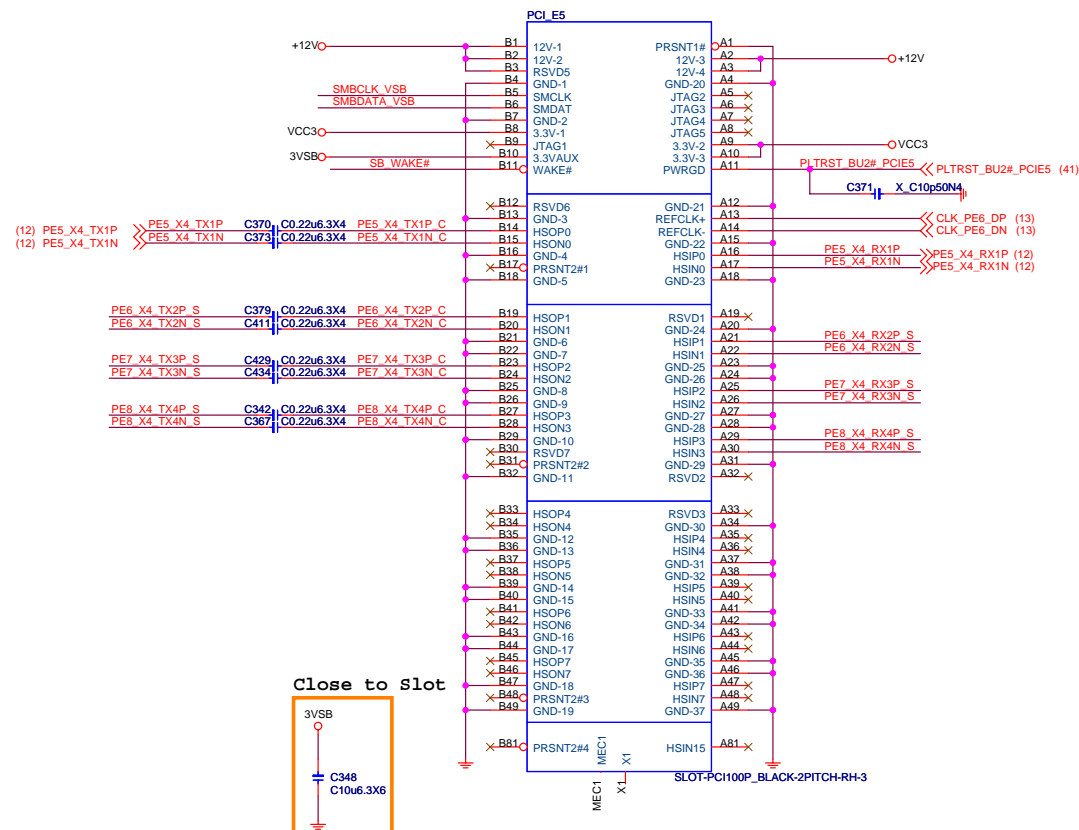
```
(15,19,20,22,46) SMBCLK_VSB
(15,19,20,22,46) SMBDATA_VSB
(15,20,22,25,26,33,35) SB_WAKE#
```

 SMBCLK\_VSB  
 SMBDATA\_VSB  
 SB\_WAKE#

PCI\_Express X4 Slot

```
support max speed GEN3
```

Black

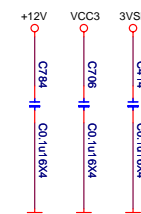


Close to Slot

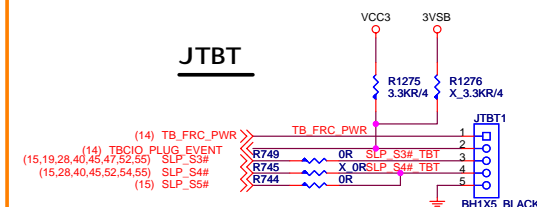


2015.05.04 Add for improve 5VDUAL Drop issue.

```
EMI:close
pin
```



JTBT

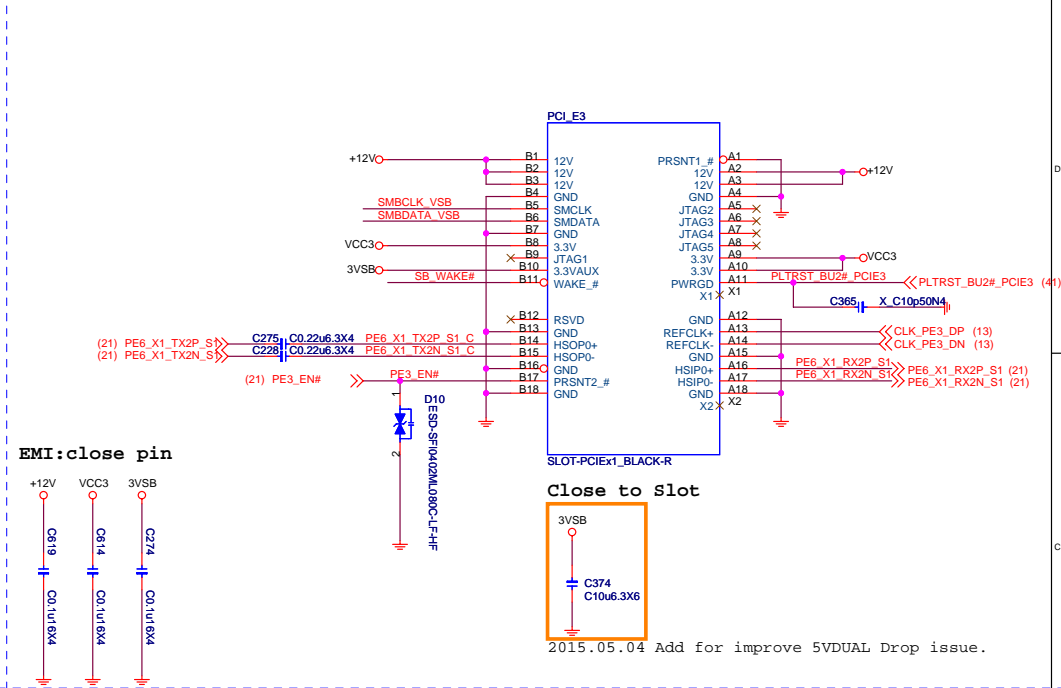
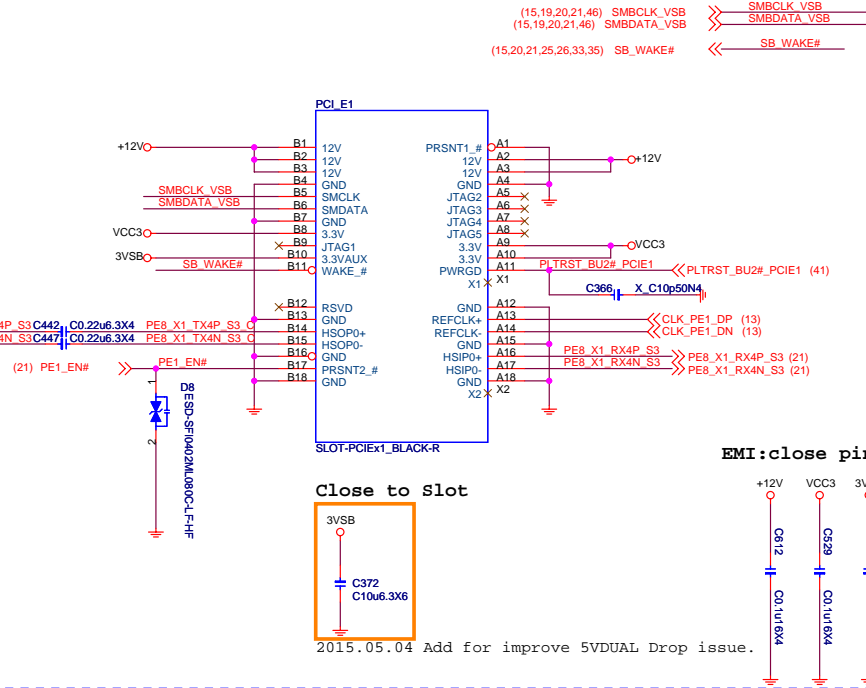


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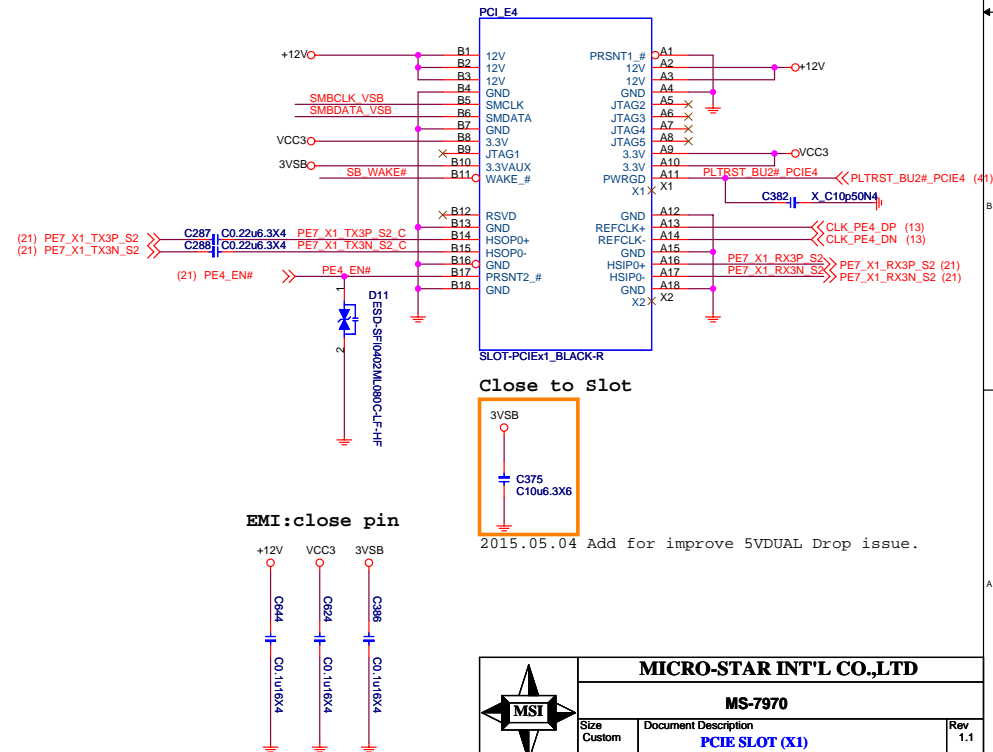
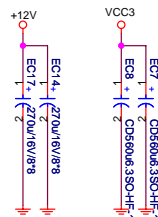
## PCIE(X1) \*3 PCIE(X4)\*1 PCIE(X16)\*1

3.3Vaux:0.375\*5=1.5A(wake)

0.02\*4=0.1A(no wake)

VCC3:3\*5=15A

+12V:0.5\*3+2.1+5.5=9.1A

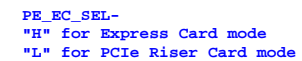
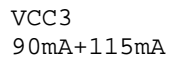


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CLK100SEL-  
 "H" for PECLK input only  
 "L" for PECLK & PCICLK input

TEST\_EN-  
 "H" for Test Mode Enable  
 "L" for Test Mode Disable

```
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable
```

```
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
```

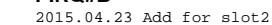


**MICRO-STAR INT'L CO.,LTD**

MS-7970

Size Custom	Document Description <b>PCIE to PCI-ASM1083</b>	Rev 1.1
Date: Thursday, July 23, 2015		Sheet 23 of 63






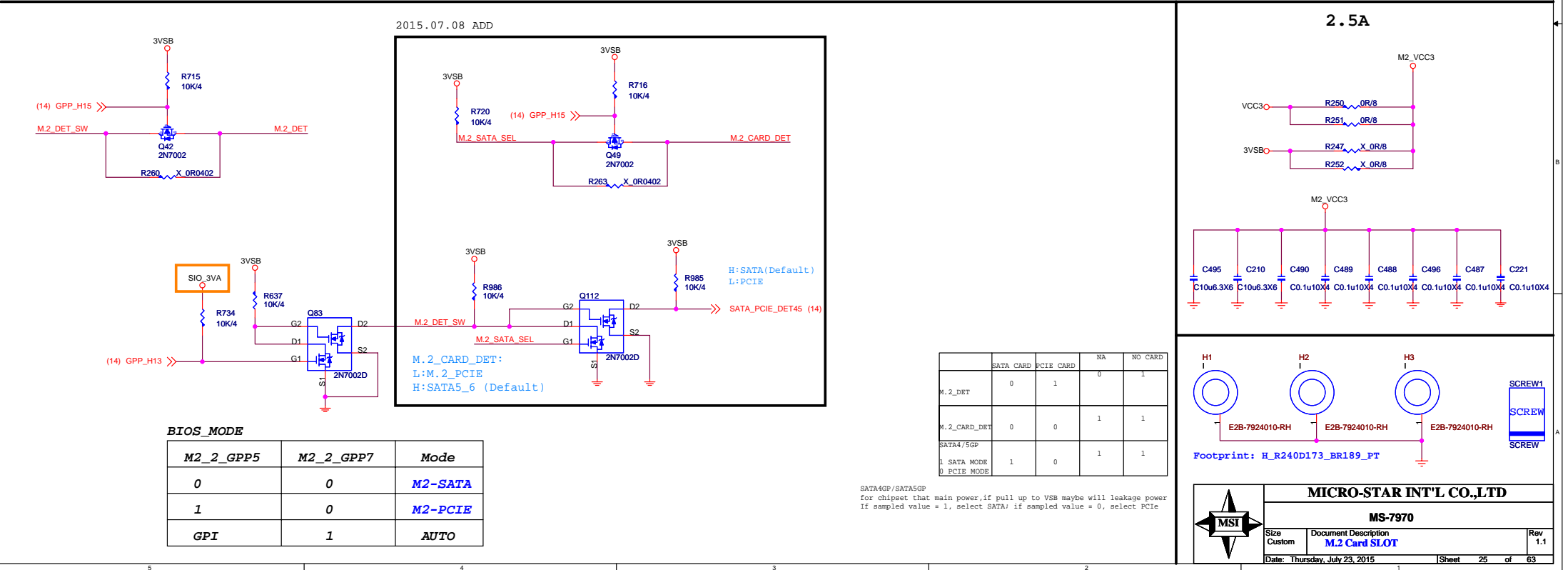
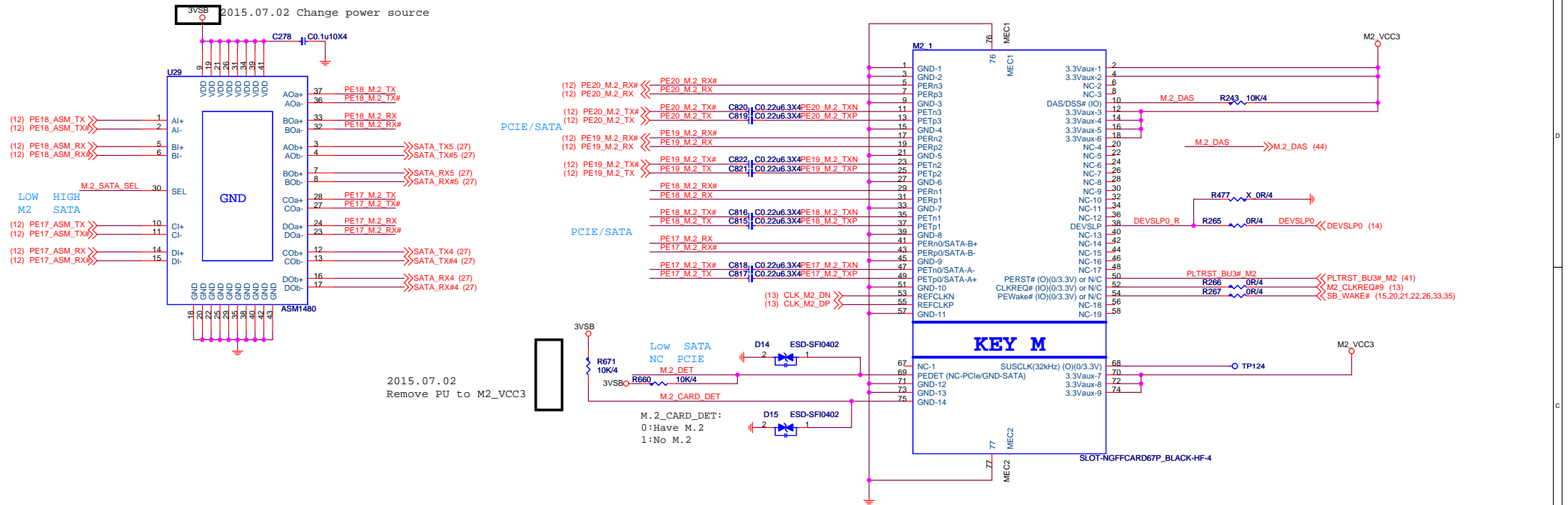
(23) PREQ#2 PREQ#2 R488 8.2KR1%  
(23) PREQ#1 PREQ#1 R668 8.2KR1%  
(23) PGNT#1 PGNT#1 R669 8.2KR1%  
(23) PGNT#2 PGNT#2 R670 8.2KR1%

(23) PIRO#B PIRO#B R491 8.2KR1%  
(23) PIRO#A PIRO#A R683 8.2KR1%  
(23) PIRO#C PIRO#C R84 8.2KR1%  
(23) PIRO#D PIRO#D R685 8.2KR1%

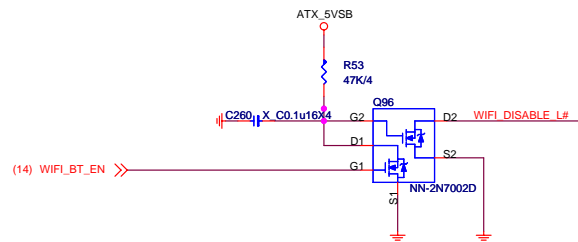
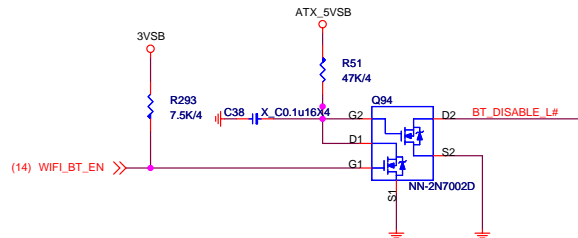
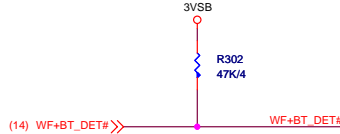
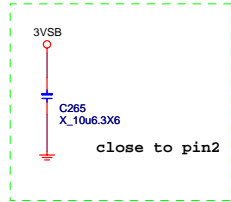
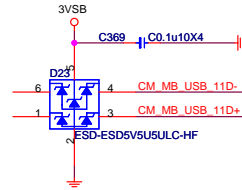
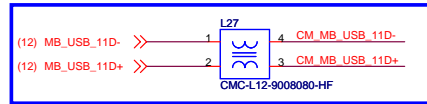
(23) PREQ#0 PREQ#0 R411 8.2KR1%  
(23) PGNT#0 PGNT#0 R410 8.2KR1%

	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7970</b>		
	Size Custom	Document Description <b>PCI SLOT</b>	Rev 1.1
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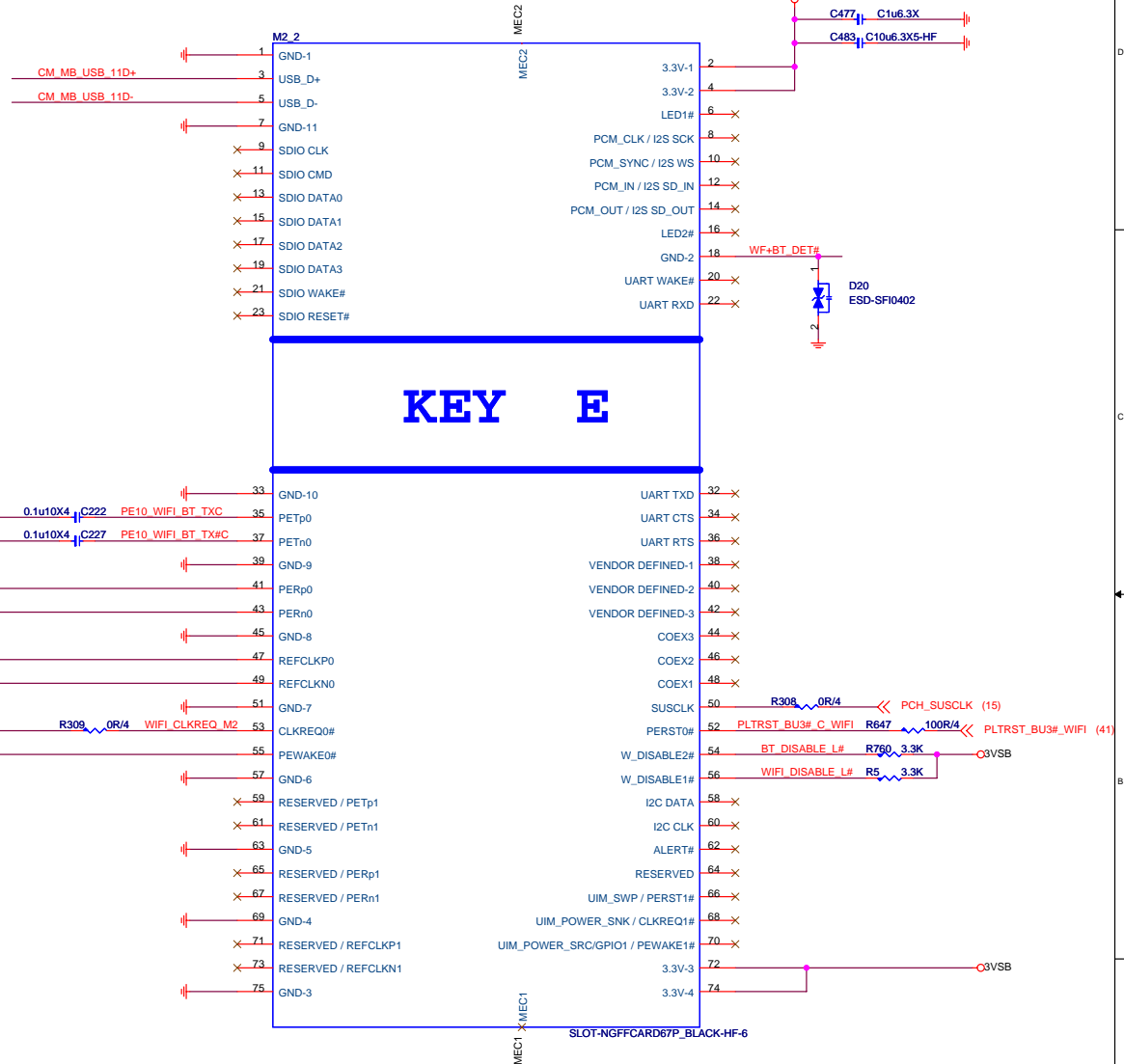
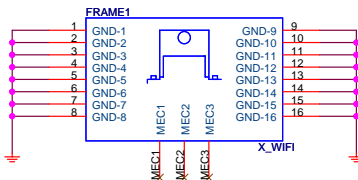
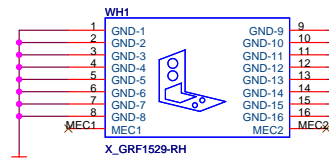
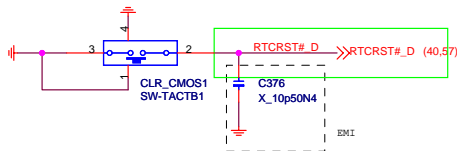








Clear CMOS Button





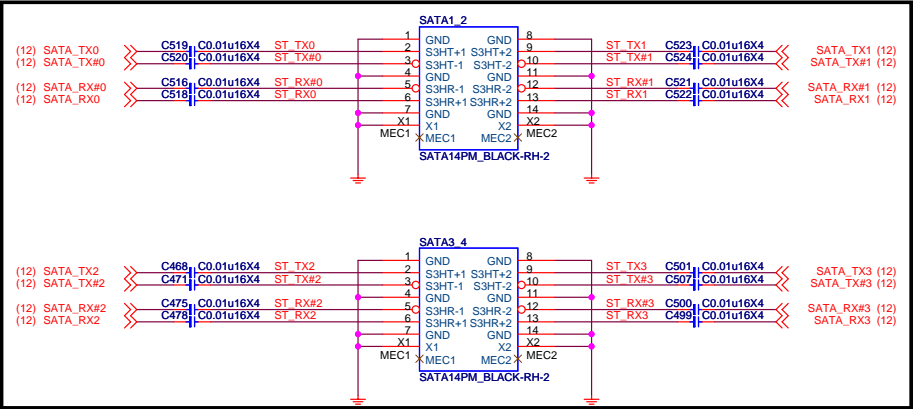
2015.05.12 Remove SE Re-Driver



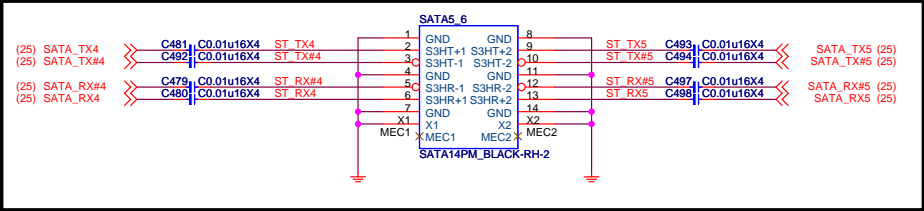
2015.07.02 Remove SE connector



2015.07.02 Modify SPEC

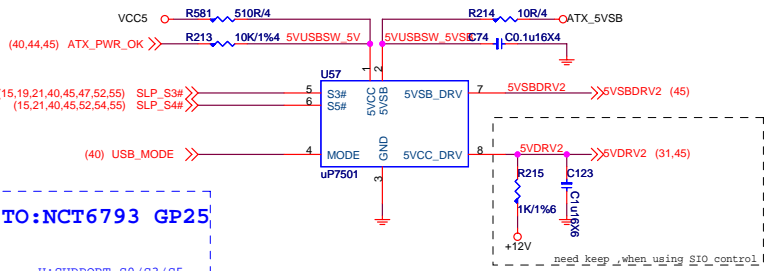


2015.05.13 Change to 90 degree



MICRO-STAR INT'L CO.,LTD			
MS-7970			
Size	Document Description		Rev
Custom	SATA Express/SATA Connector		1.1
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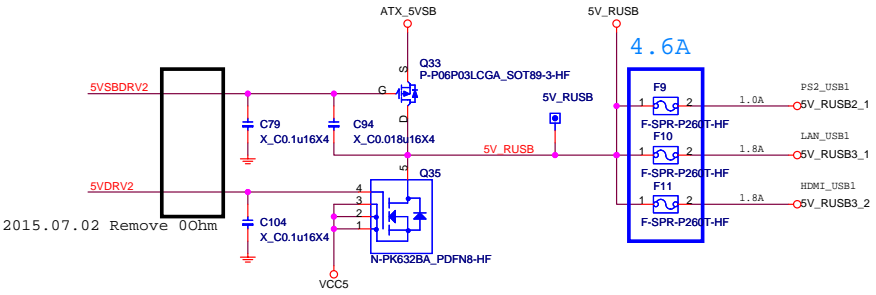




TO:NCT6793 GP25

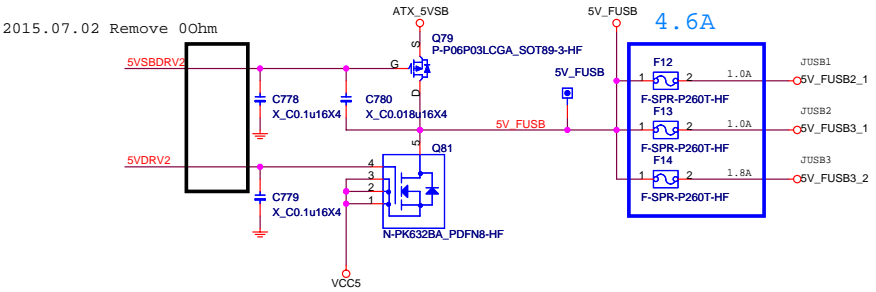
H:SUPPORT S0/S3/S5  
L:SUPPORT S0/S3

5VDRV2, 5VSBDRV2 width 12mil,  
Do NOT route near the edge of a board.



2015.07.02 Remove 00hm

need confirm C780 value



2015.07.02 Remove 00hm

P-MOS  
D03-06P0319-N03

N-MOS  
D03-510BA0C-N03  
D03-3056M00-U47  
D03-4C05N03-005  
D03-3830D09-N47  
D03-632BA0C-N03

D08-2000300-P16 (Itrip=3.5A; 0.003ohm)  
D08-0300700-P16 (Itrip=2.6A; 0.015ohm)

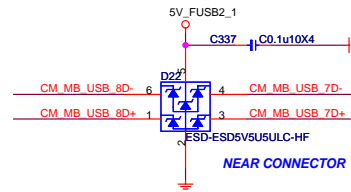
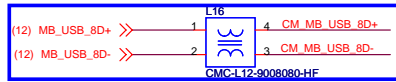
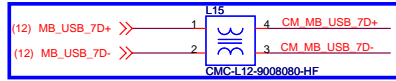
Front USB2.0 Voltage Drop Fail.



MICRO-STAR INT'L CO.,LTD		
MS-7970		
Size	Document Description	Rev
Custom	USB POWER-MP1495/UP7501	1.1
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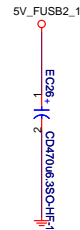
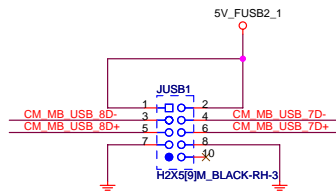
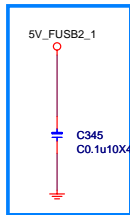
# FRONT USB PORT 7,8



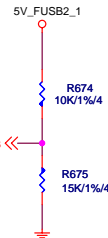
NEAR CONNECTOR

1.0A

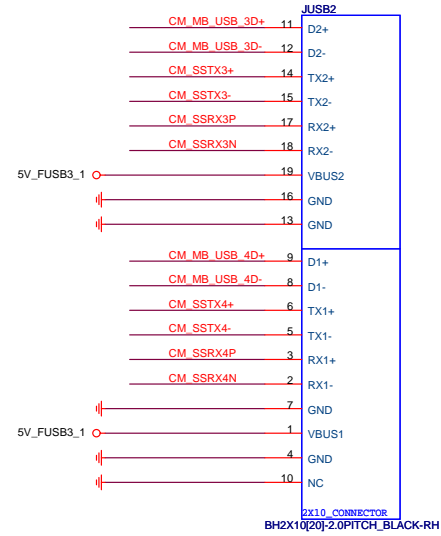
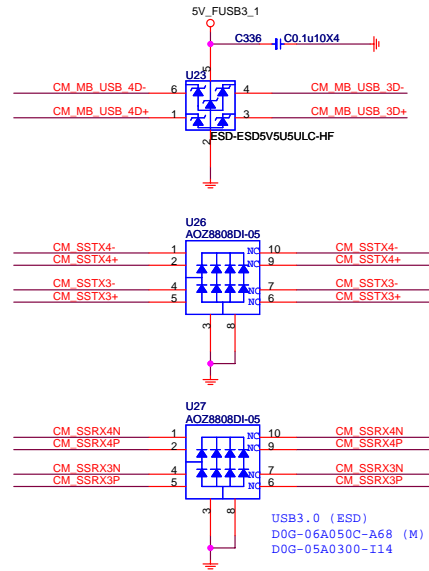
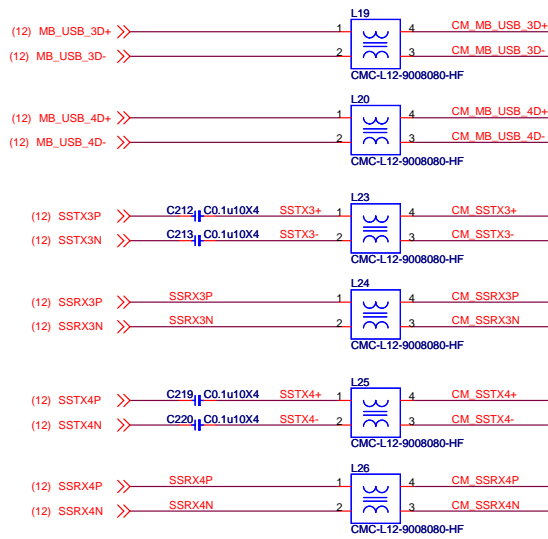
EMI Cap near Connector.



(14) OC#3

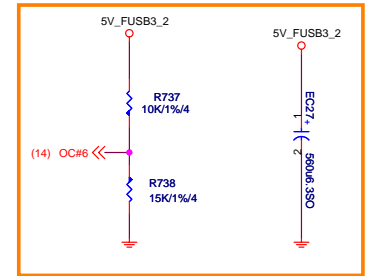
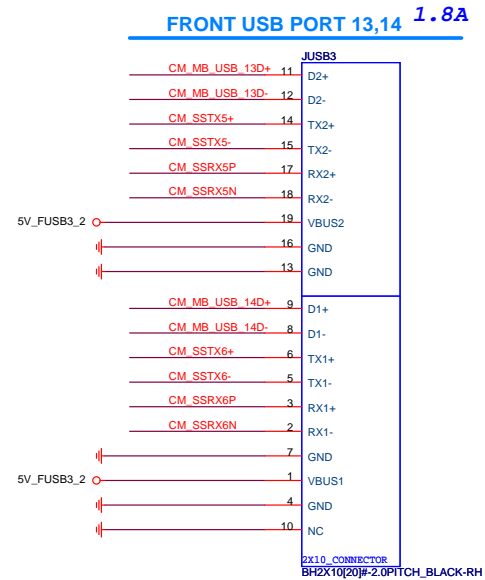
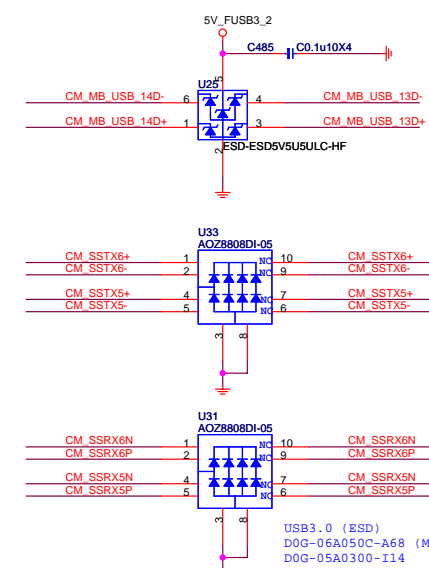
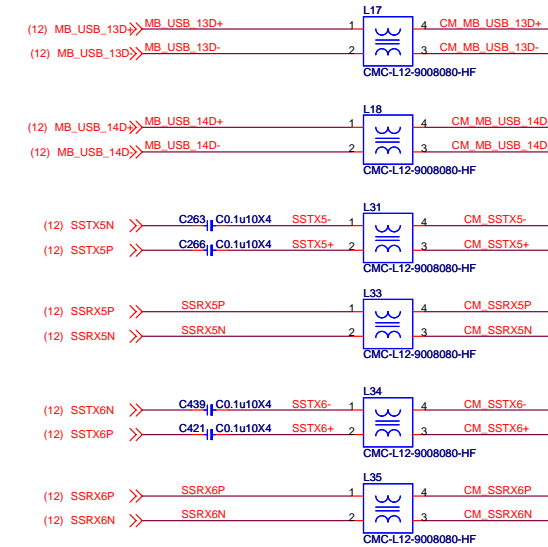
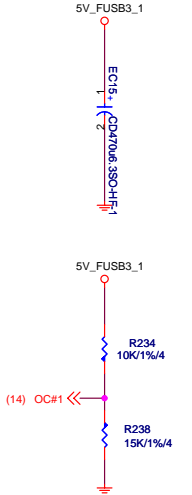
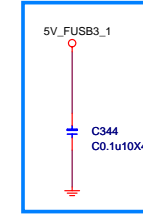




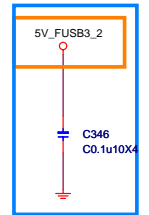


1.8A

EMI Cap near Connector.



EMI Cap near Connector.



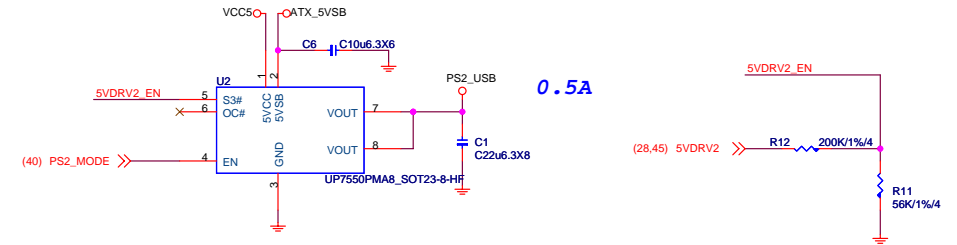
MICRO-STAR INT'L CO.,LTD

MS-7970

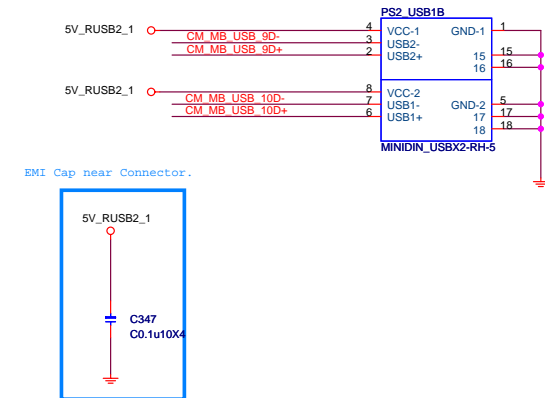
Size	Document Description	Rev
Custom	Front USB3.0	1.1
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**USB MODE**

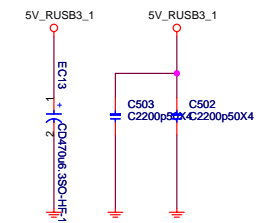
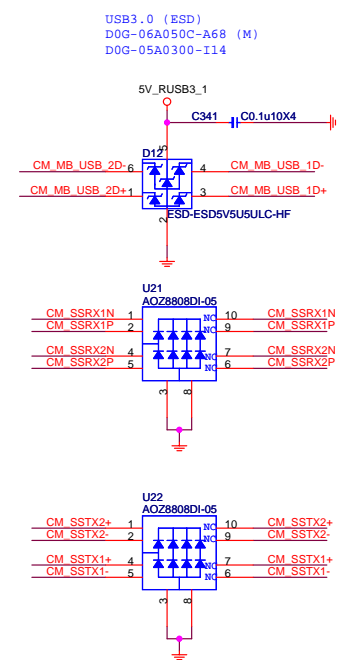
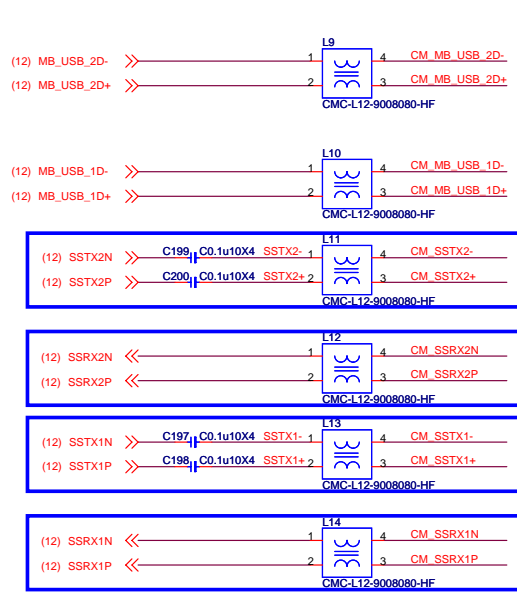


$1.0A$

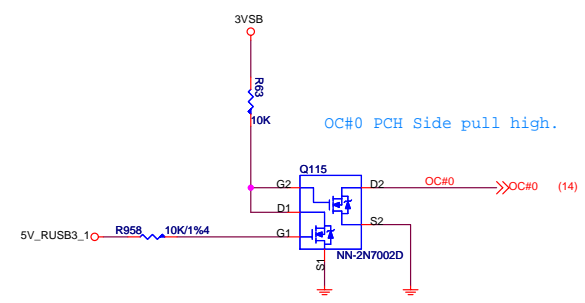
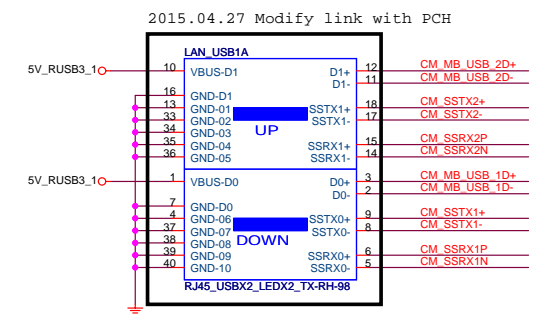
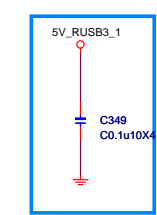


Size Custom	Document Description <b>Rear I/O PS2/USB2</b>	Rev 1.1
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EMI Cap near Connector.



From ASM1142.

From ASM1142.

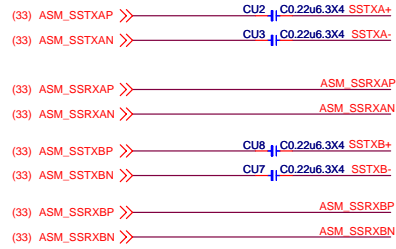
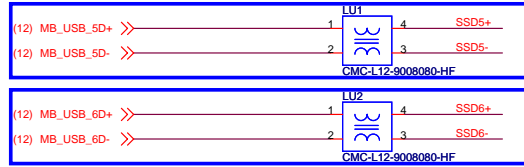




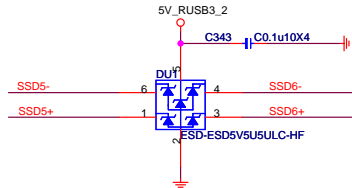


# Rear USB3 CONN

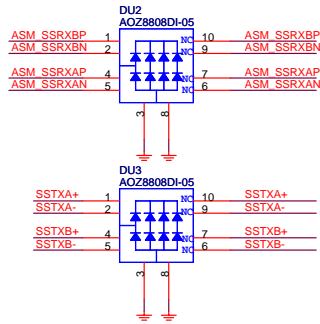
Important--  
If USB3.0 signal connect to front pin header,  
please must less than 1.5 inch,short trace  
has better eye diagram with some bad fly cable by SI customer.



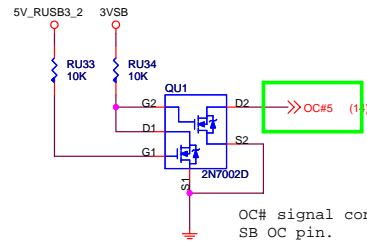
USB2.0  
D0G-0200529-A68 Main  
D0G-0100619-I05 AVL



## ESD Protection NEAR CONNECTOR

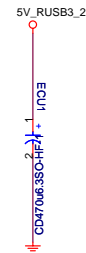


USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL

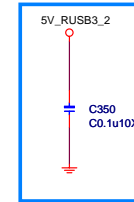


OC# signal connect to  
SB OC pin.

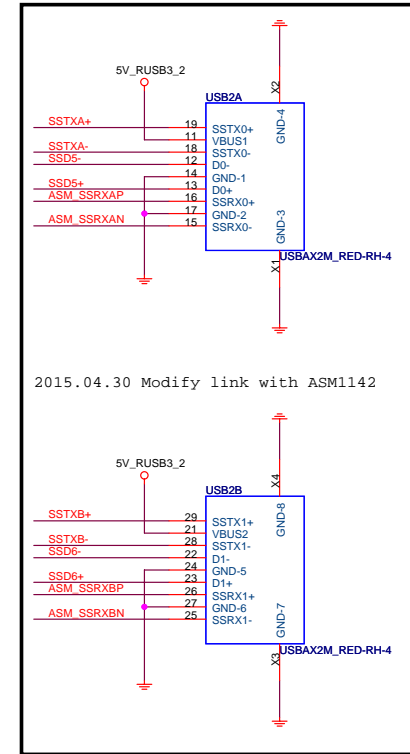
min 80mil.  
1.8 A



EMI Cap near Connector.



1.8A



2015.04.30 Modify link with ASM1142



MICRO-STAR INT'L CO.,LTD

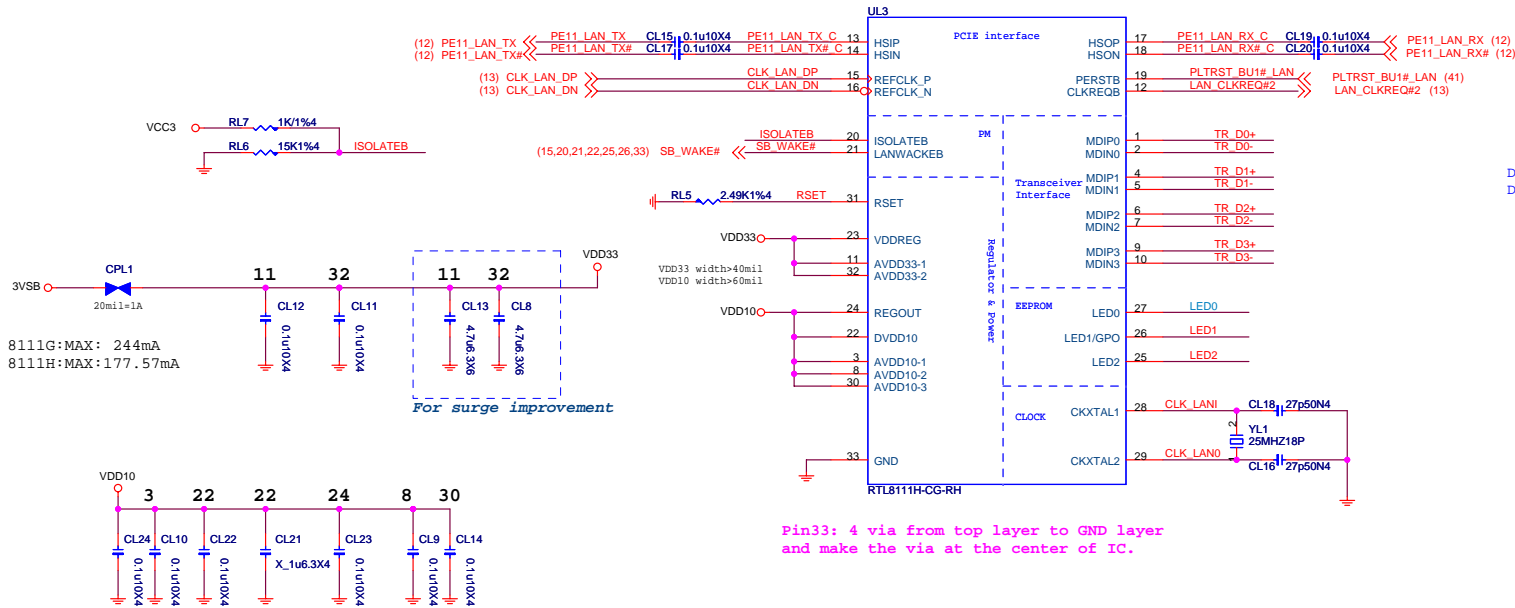
MS-7970

Size	Document Description	Rev
Custom	Rear USB3.1 Connector	1.1
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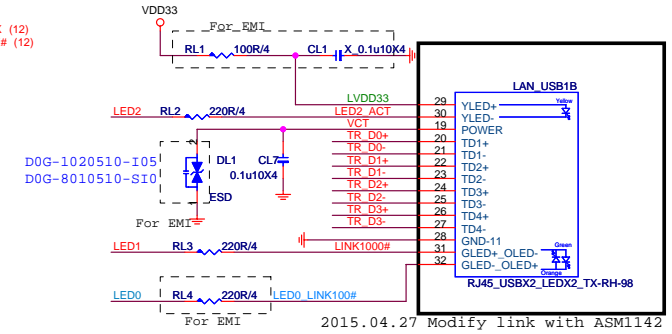


## RTL8111G/RTL8111H Giga LAN

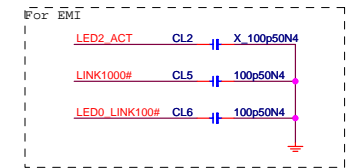
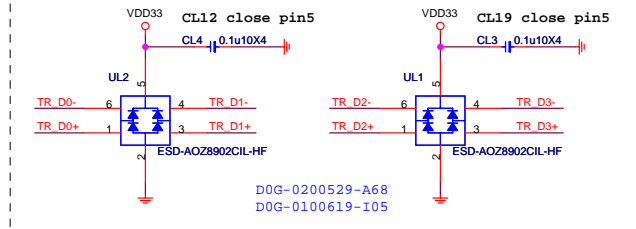
8111H:B06-08111CC-R09  
8111G:B06-081116C-R09



## LAN Connector



Update moduale 2015.05.25

ESD Protect  
UL2&UL3 close to connector

## 8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

## 8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



MICRO-STAR INT'L CO.,LTD

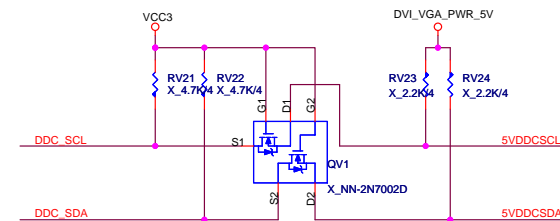
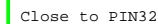
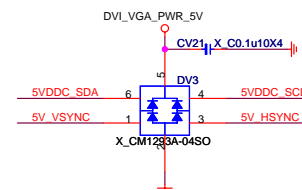
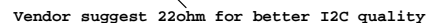
MS-7970

Size	Document Description	Rev
Custom	LAN Killer E2205	1.1
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If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



**MS-7970**

Size Custom	Document Description <b>VGA Connector</b>	Rev 1.1
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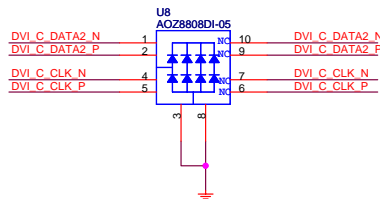


# VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

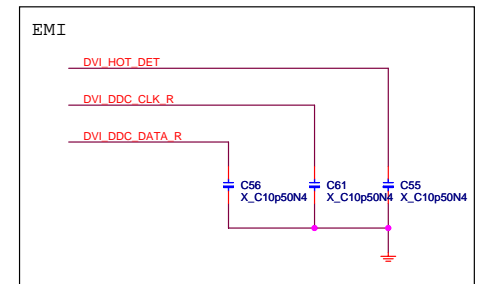
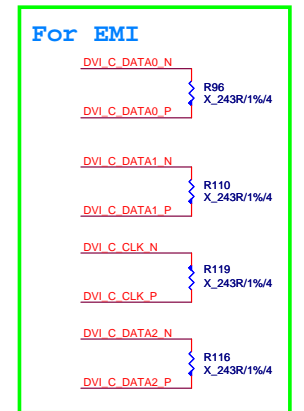
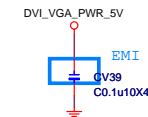
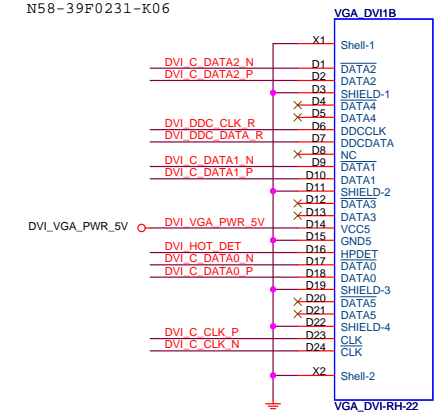
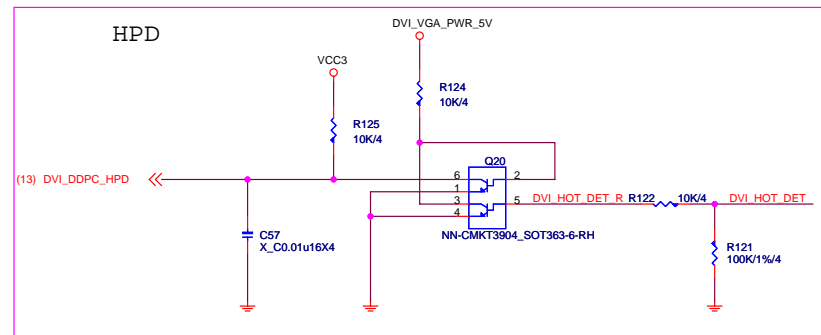
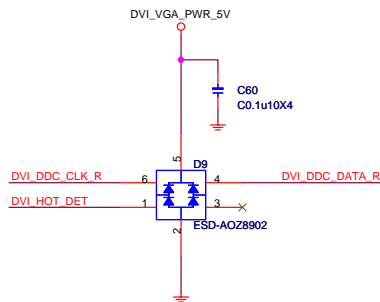
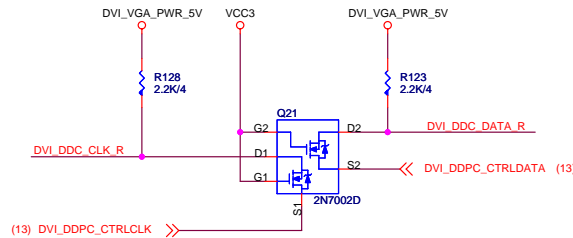
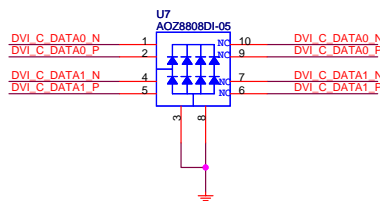
Check MSI PN  
N58-39F0231-K06



U26 AVL:D0G-05A050C-005  
D0G-06A050C-A68

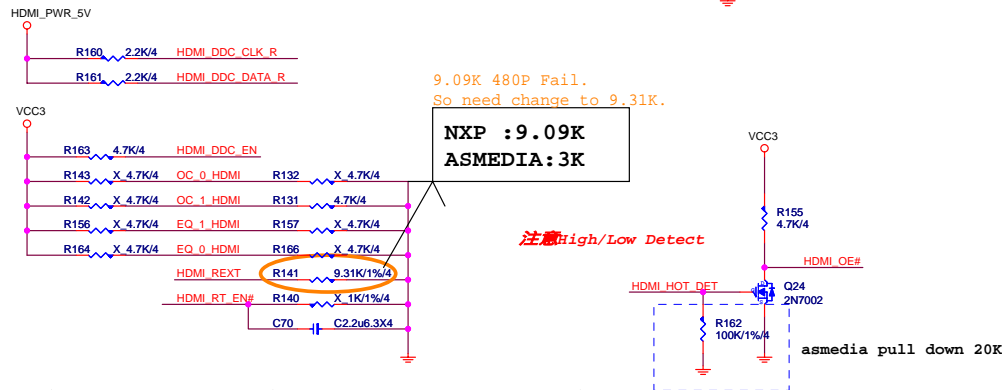
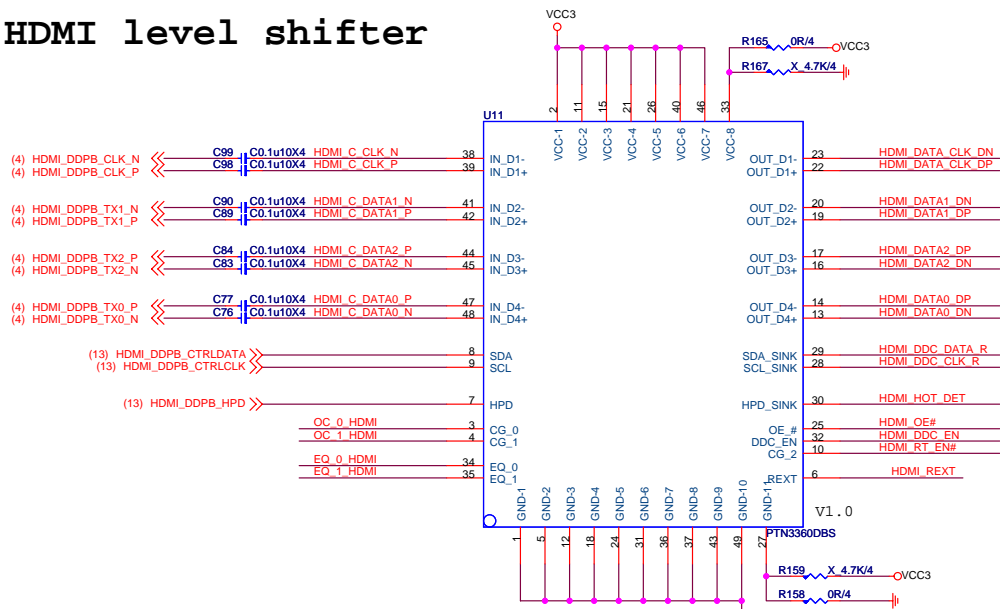


U27 AVL:D0G-05A050C-005  
D0G-06A050C-A68





## HDMI level shifter



	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

generalization		note
PC1, PC0		
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

internal pull-up at  
~500K ohm.  
internal pull-down at ~500K ohm.

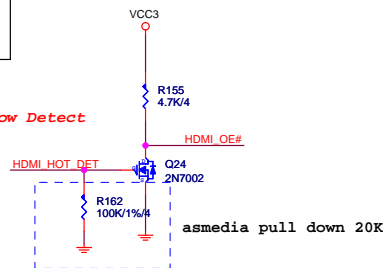
internal pull-down at ~500K ohm.

internal pull-down at ~200K ohm;  
5V tolerant.

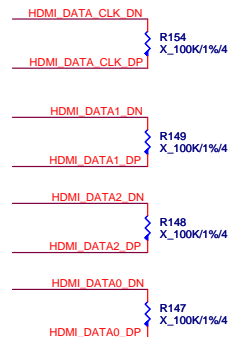
internal pull-down at ~500K ohm.

**analog current generation.**

note



EMI



EMI cap.

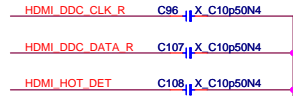
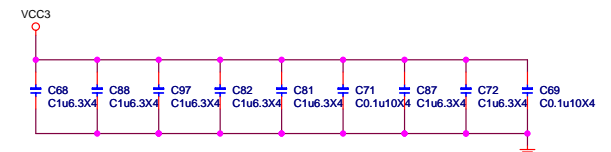
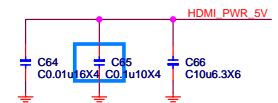
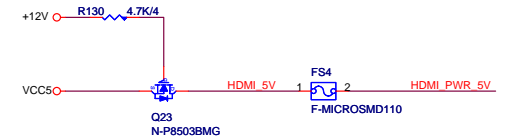
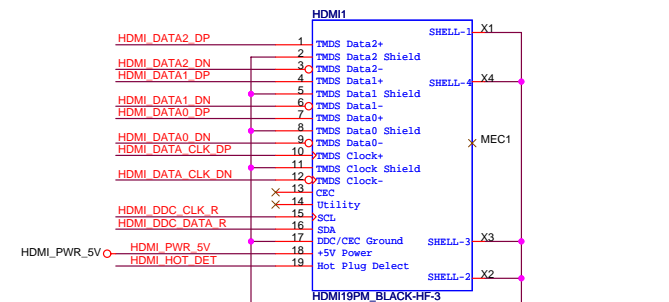


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCB Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	THDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	THDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	THDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	THDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	THDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	THDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	THDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	THDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI5_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMI5_CTRL_DATA		



**MICRO-STAR INT'L CO.,LTD**

MS-7970

Size	Custom
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Document Description  
**HDMI Connector**

Rev	
1.1	

Date: Thursday, July 23, 2015	1	Sheet	38	of	63
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Type B:  
ALC892/887

2015.04.24 Modify from  
ALC1150 to ALC892

(13) AZ\_SDOUT  
(13) AZ\_SDI0  
(13) AZ\_SYNC  
(13) AZ\_RST#  
(13,58) AZ\_BITCLK

CA29  
X\_10P50N4

REGREF

CA30  
10u6.3X6

45.8mA

CA26  
X\_0.1u16X4

CA28  
10u6.3X6

Closed Codec

CA26.CA28 close to Pin27

EMI

CA13 X\_C0.1u16X6  
CA42 X\_C100p16X6

GPA3 X COPPER  
GPA4 X COPPER

SENSE A  
SENSE B

RA22 5.1K1/4  
RA19 10K1/4  
RA20 20K1/4  
RA21 39.2K1/4

SENSE B  
RA27 10K1/4

DN010

Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)

All components are mounted by PM request

VCC3

RA37 10K/4

EAPD RA38 1K/4

Digital

Analog

MUTE RA39 1K/4

RA44 1K/4

NN-HBN251556R

CA36 0.1u10X4

CA37 22u6.3X8

CA38 10u6.3X6

CA39 10u6.3X6

CA40 10u6.3X6

CA41 10u6.3X6

CA42 10u6.3X6

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CA

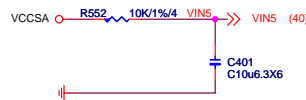
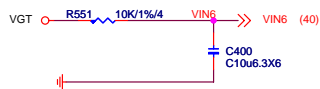
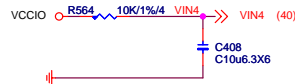
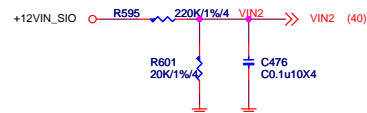
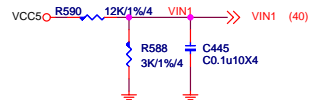
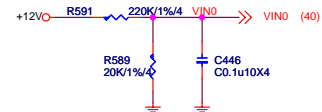
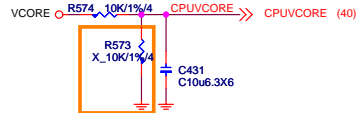
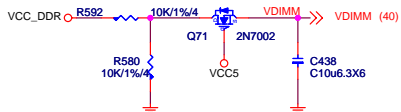






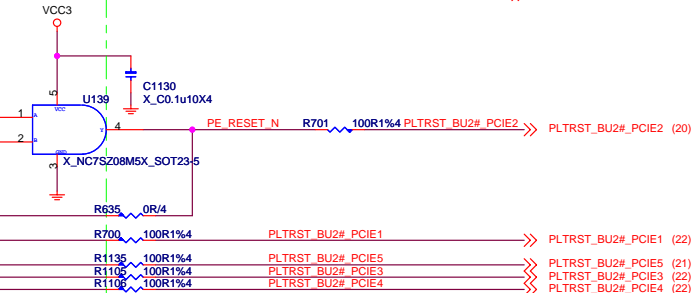
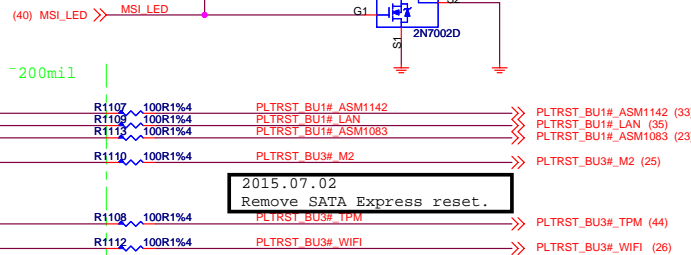
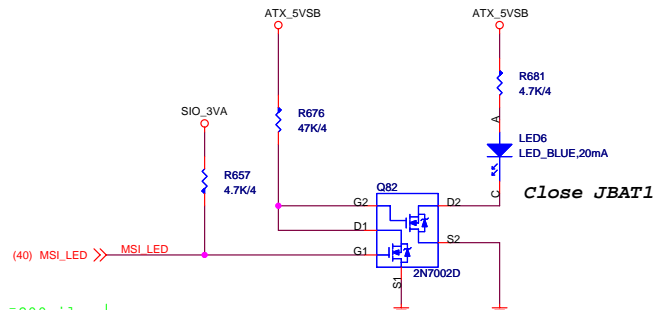
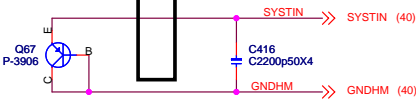
## HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



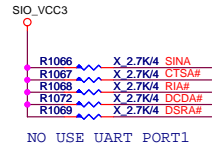
## Thermal Monitor

2015.07.02  
Remove Thermistor.

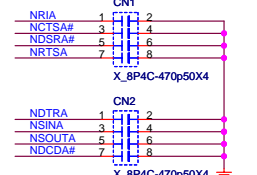
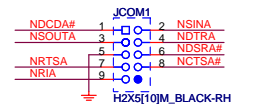
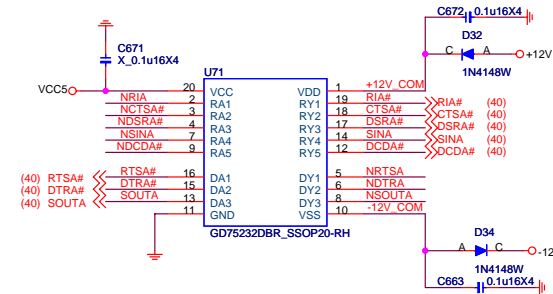


## SERIAL PORT 1

2015.04.24 Add

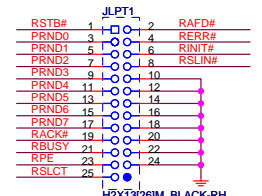
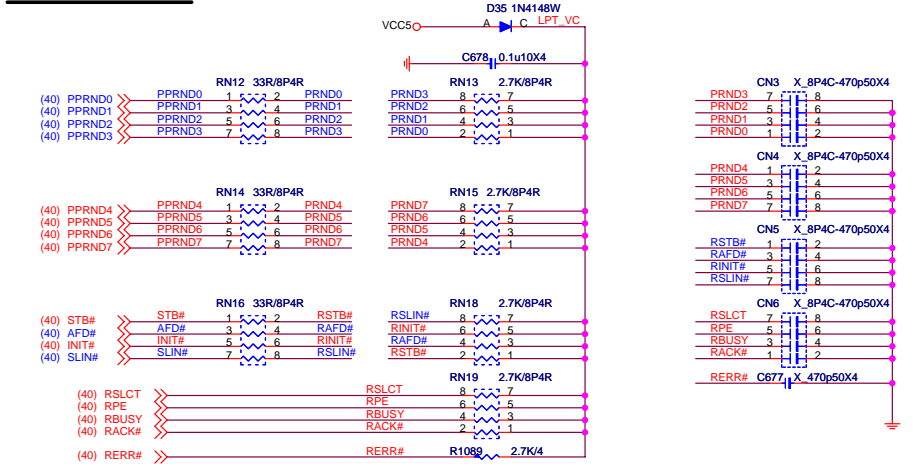


NO USE UART PORT1



## PARALLAL PORT

2015.04.24 Add



N31-2131151-H06 : 2.0mm  
N31-2131131-H06 : 2.54mm



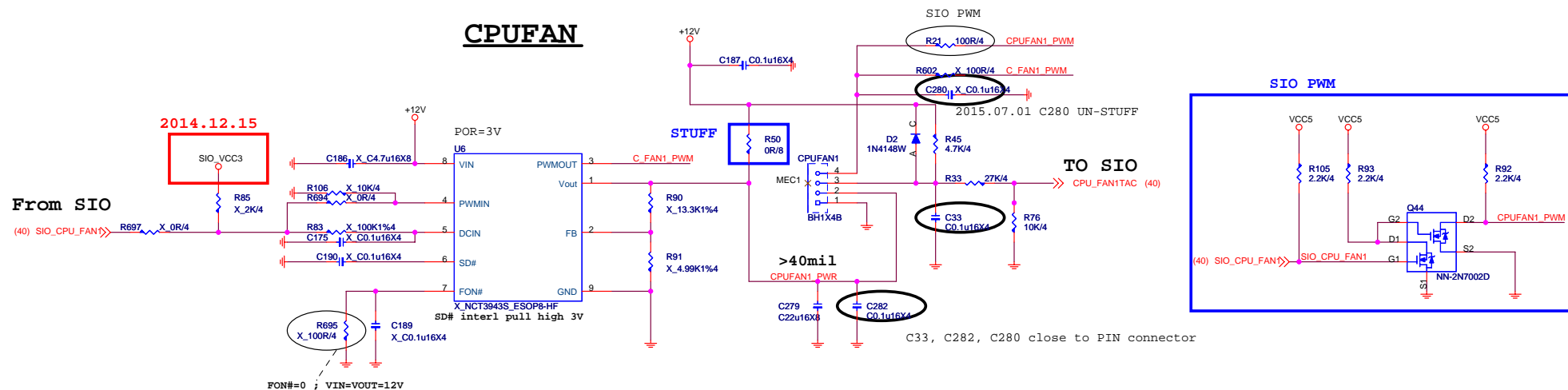
MICRO-STAR INT'L CO.,LTD

MS-7970

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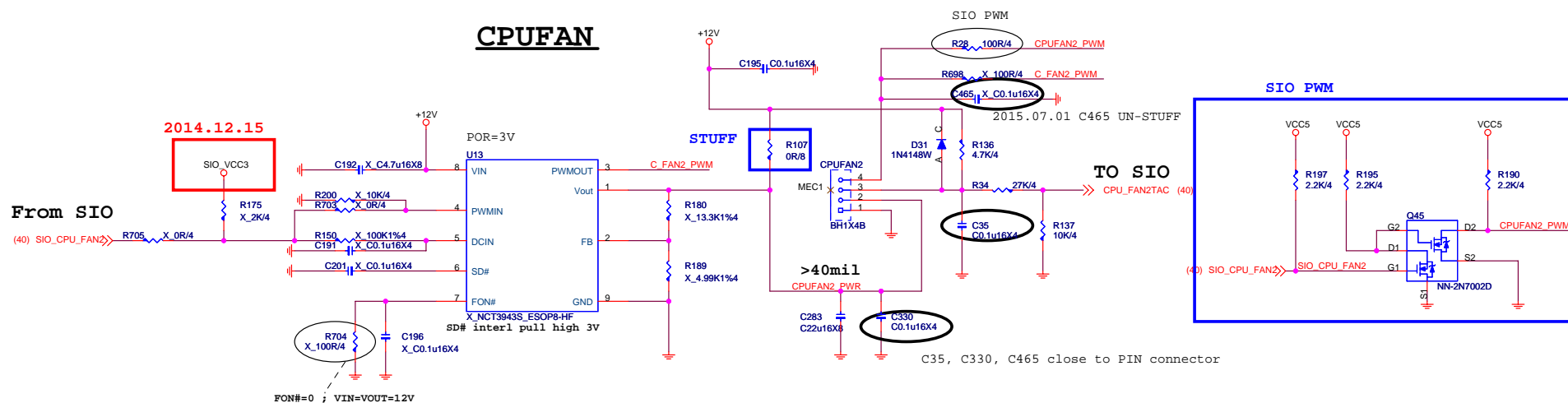
# Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



## WITHOUT CUT POWER

BOM OPT	R602	R21	R105	R93	R92	Q44	R697	R85	R106	R694	R83	C175	R695	C186	U6	R90	R91	R50
SIO PWM	X	O	O	O	O	O	X	X	X	X	X	X	X	X	X	X	X	O

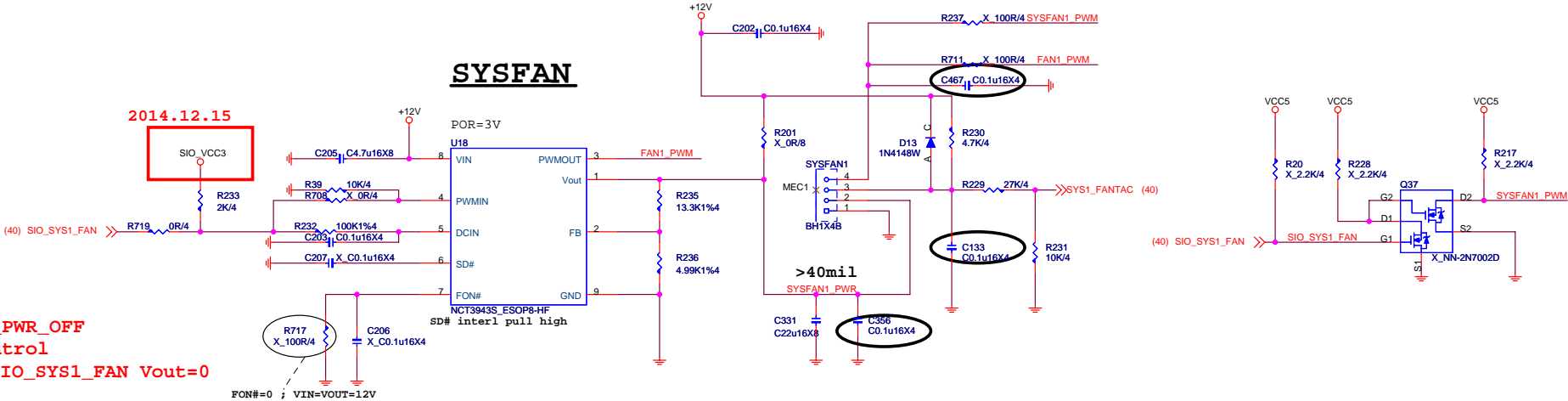
# Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)



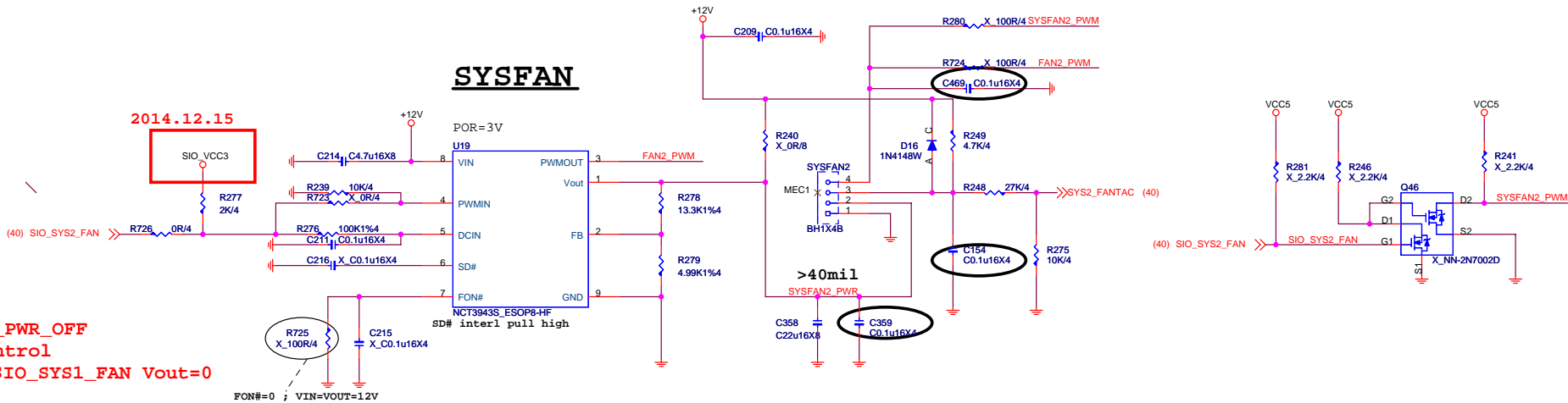


Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)

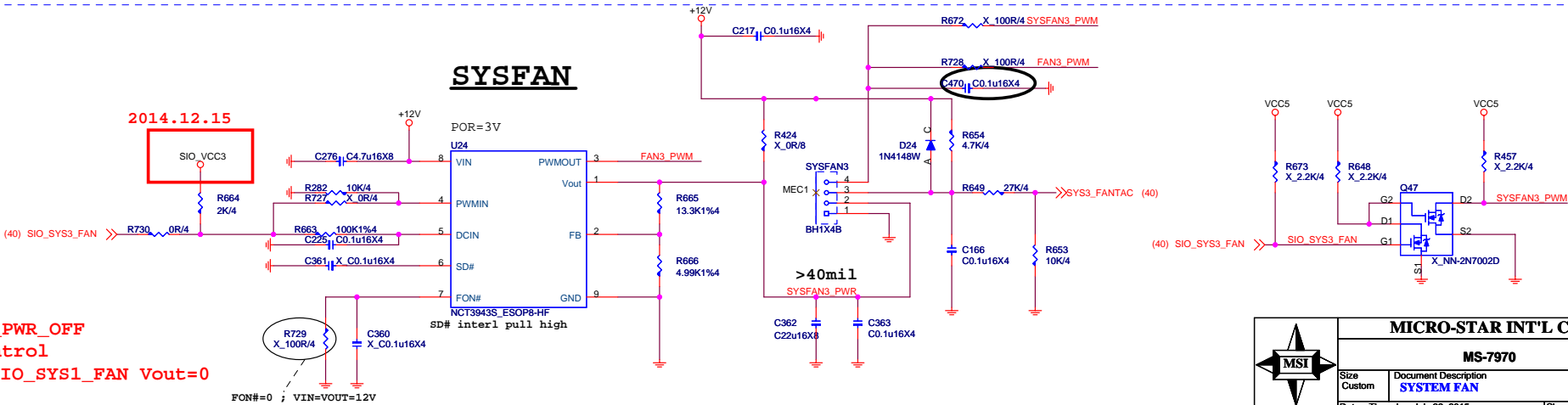
SYSFAN



SYSFAN



SYSFAN

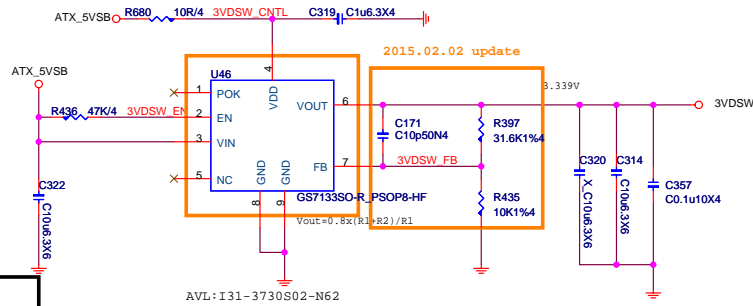








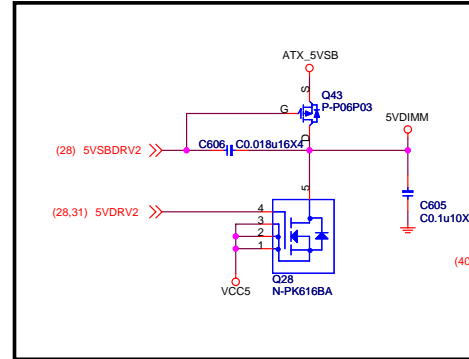
## 3VDSW



2015.05.25 Remove CUT\_VBAT

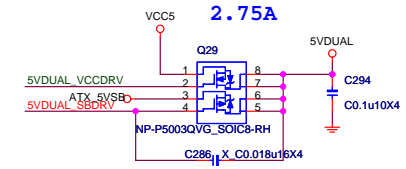
## 5VDIMM FOR 5VDUAL

2015.05.19 Power source change with USB.



## 5VDUAL

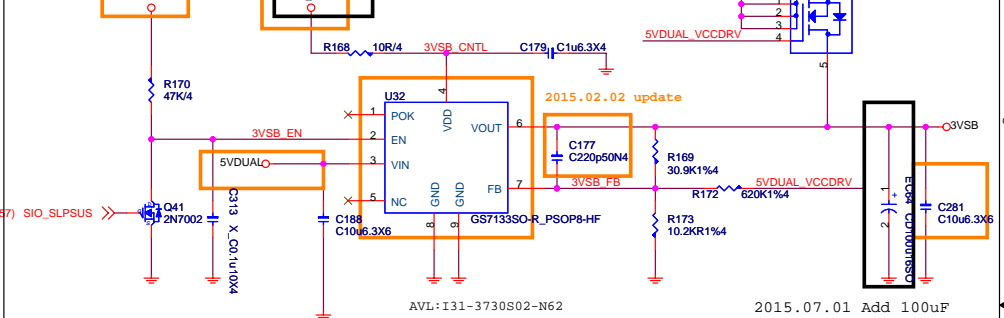
5VDUAL is power source of PCH\_1VSB.



## 3VSB cost down

all PCH Primary Rails ramp up within 20ms.

2015.05.04 Change power source



2015.05.25 Remove CUT\_VBAT to CUT\_VBAT\_3VSB  
VFB=3.224V for S0->S3 3VSB voltage raise & ATX\_5VSB drop.

## CUT\_VBAT

2015.05.25 Remove CUT\_VBAT to 3VDSW

CUT 3VDSW

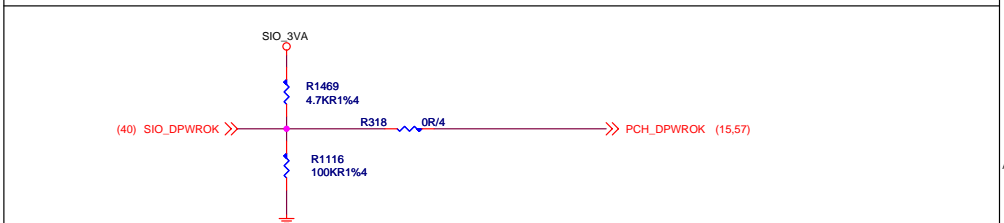
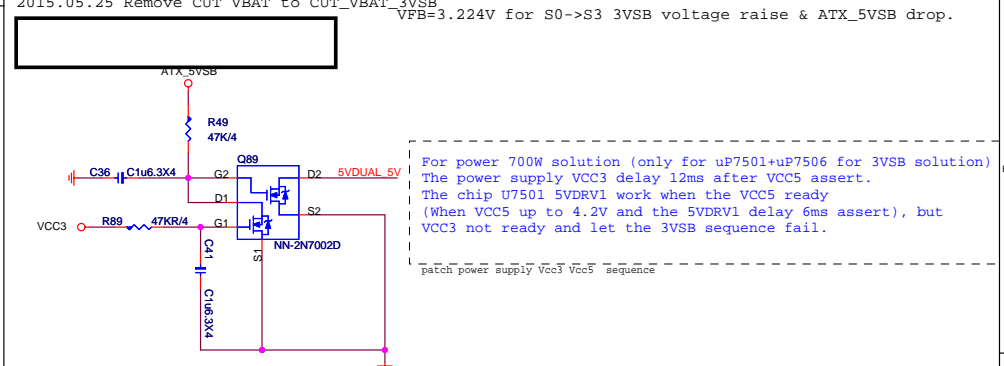
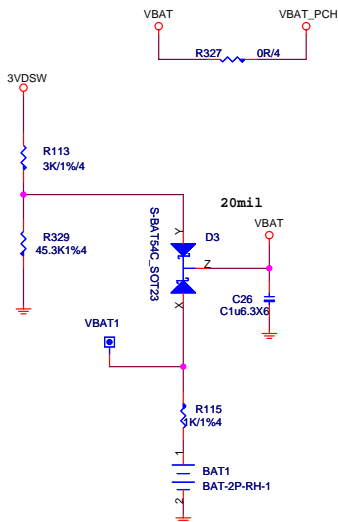
2015.05.25 Remove CUT\_VBAT to CUT\_VBAT\_3VSB

CUT 3VSB

2015.05.25 Remove CUT\_VBAT to CUT\_1VSB\_EN

CUT PCH\_1VSB

CRB

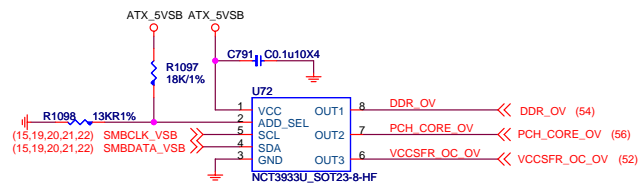




Remove Cut Power.

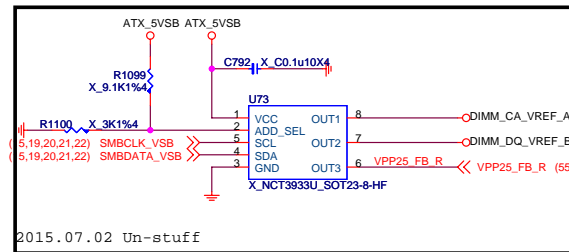
### UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=1.3K



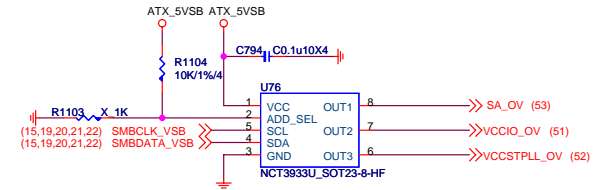
### UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



### UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



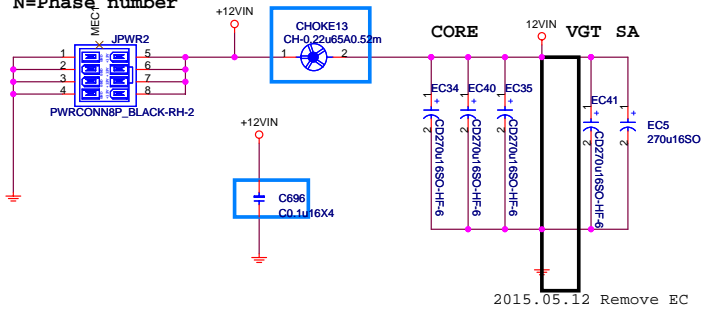
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MS-7970

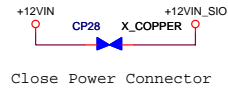
Size	Document Description	Rev
Custom	OV-NCT3933/GPIO-NCT5605	1.1
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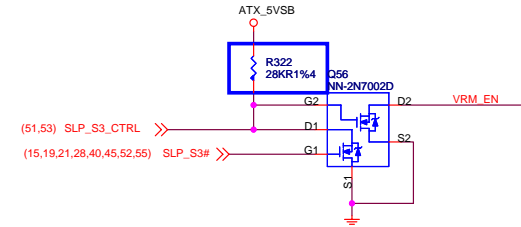
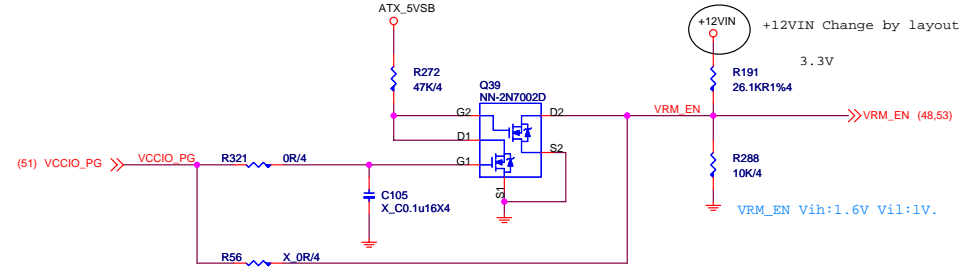
$I_{rms} = I_{out} * \sqrt{D/N * (D)^2}$   
 $D = V_{out}/V_{in}$   
 $N = \text{Phase number}$



$I_{ripple} = 23.097A$   
 $V_{CORE} = 12.47A$   
 $V_{GT} = 7.2977A$   
 $V_{CCSA} = 3.33A$

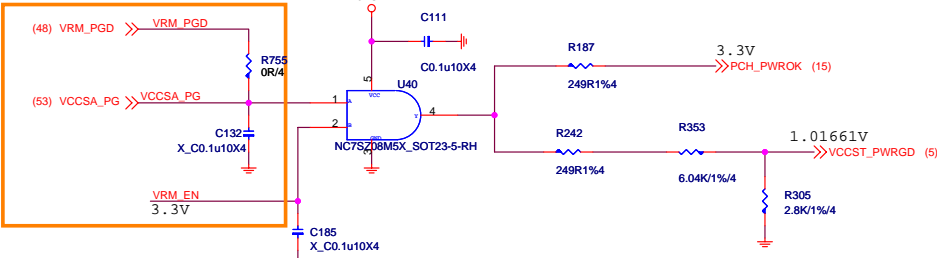


VRM\_EN Control from VCCIO\_PG

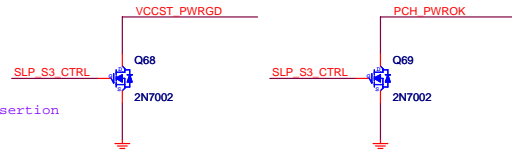


PCH\_PWROK Control from VCCIO\_PG&VCCSA  
 VCCST\_PWROK Control from VRM\_PGD

VCCSA&Vcore use same PWM IC, pull up VCC3  
 VCCSA&Vcore use different PWM IC, pull up VCCSA  
 VCCST\_PWROK can assert before or equal to PCH\_PWROK, but must never lag it.

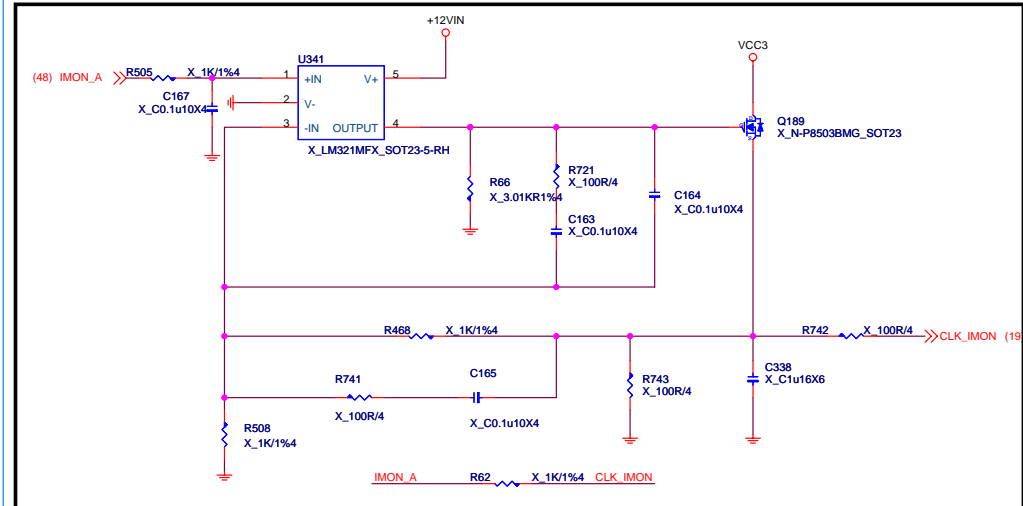


VCCIO使用NB681/685時, PIN 3V3要接外部VCC3,  
 VCCIO\_PG上升時會彈一根到0.6V,  
 所以PCH\_PWROK前端控制的VCCIO\_PG改接VRM\_EN.



For VCCST\_PWROK deassertion  
 max:1us

2015.05.22 Prevent use same IMON cause noise.



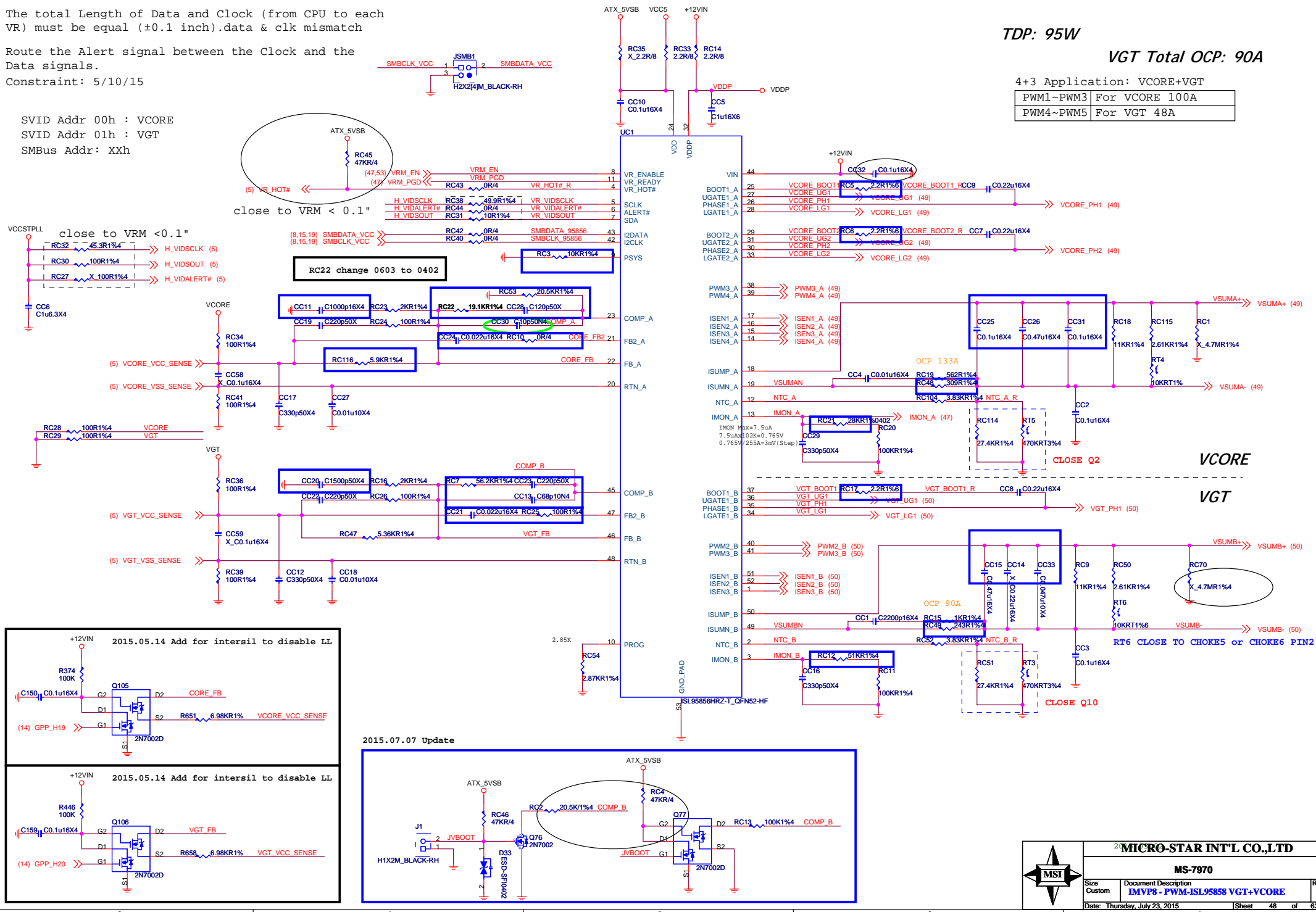


The total Length of Data and Clock (from CPU to each VR) must be equal ( $\pm 0.1$  inch). data & clk mismatch

Route the Alert signal between the Clock and the Data signals.

Constraint: 5/10/15

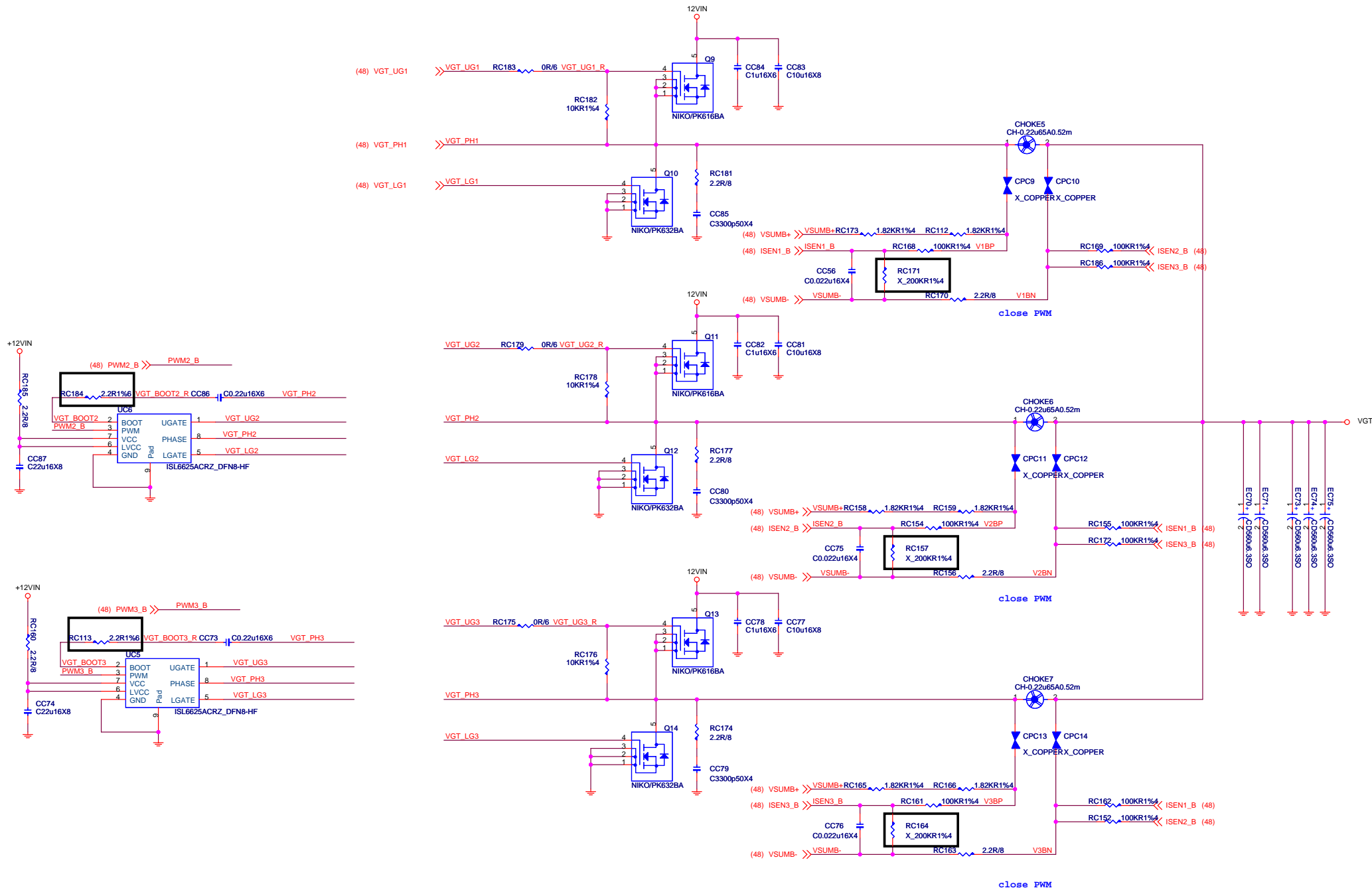
SVID Addr 00h : VCORE  
SVID Addr 01h : VGT  
SMBus Addr: XXh





[illegible]



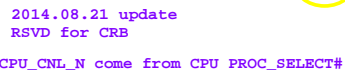




0.95V; 5.5A  
(H110 VCCIO=VCCSA)

$I_{MAX} 10A$   
 $I_{LIMIT}=10A\sim 12A$   
 $I_{OC}=I_{LIMIT}+40\%*I_{MAX}/2=12A\sim 14A.$

L04-01072H0-T15  
AVL: L04-0107800-M26



Size Custom	Document Description <b>CPU PWR_VCCIO</b>	Rev 1.1
Date: Thursday, July 23, 2015		Sheet 51 of 63



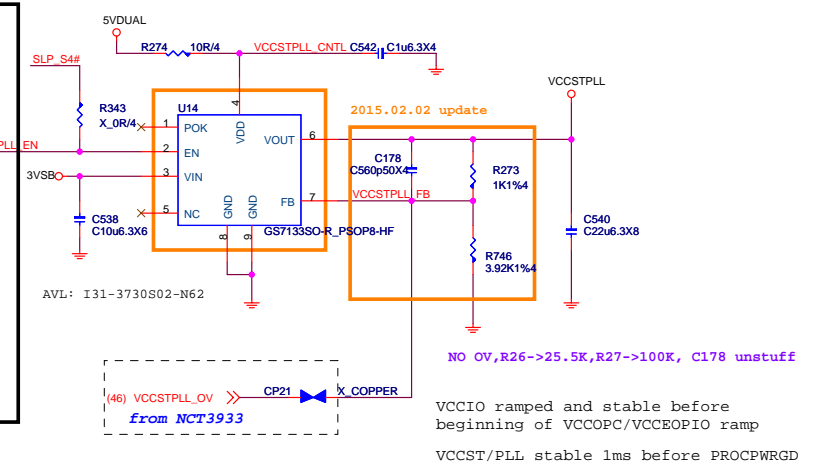
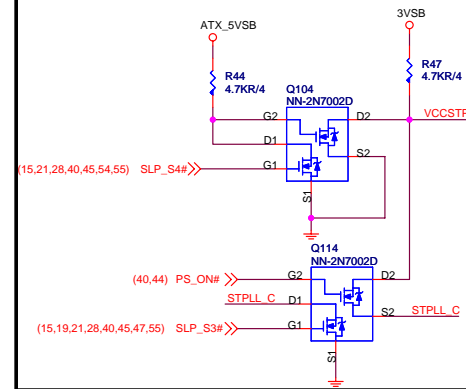
# VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO and H110

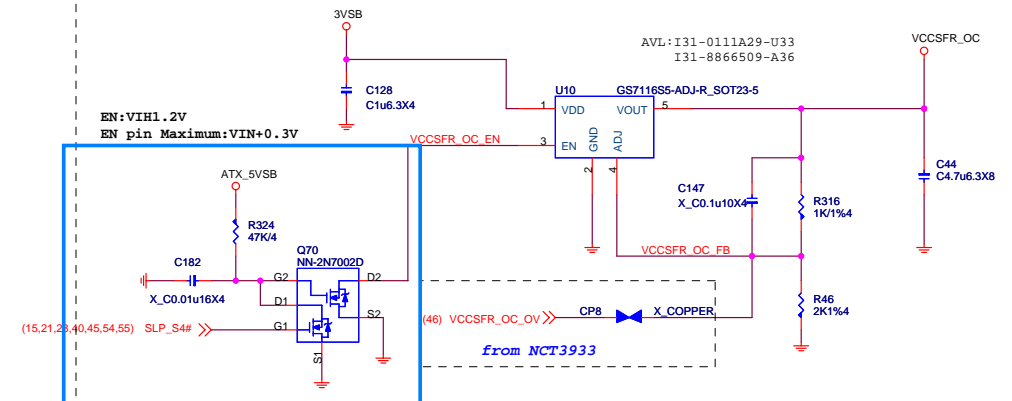
2015.05.22 Update



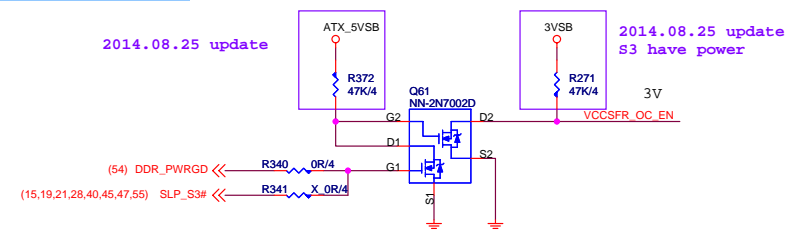
# VCCPLL\_OC

1.2V; 110mA

2014.08.21 update



2014.08.25 update



2014.08.25 update  
S3 have power

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MS-7970			
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Custom	CPU PWR ST/PLL	1.1	
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# SA Power:1.05V,12.3A

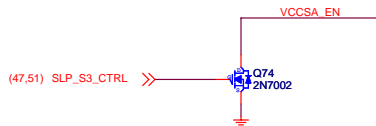
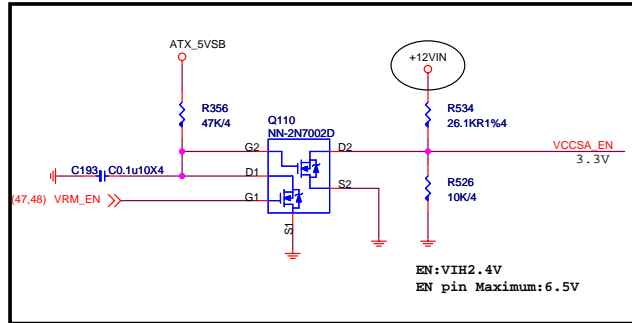
OCP = 12.3A \* 1.4 = 17.22A

Rocs(R15)=OCP\*Rdson(Low side)/10uA  
=17.22\*(3.4)mohm/10uA  
=5.854Kohm

Rocs:5.76K,OCP:  
D03-4C05N03-005 : 16.94A  
D03-632BA0C-N03 : 17.45A  
use UBIQ MOS need Check

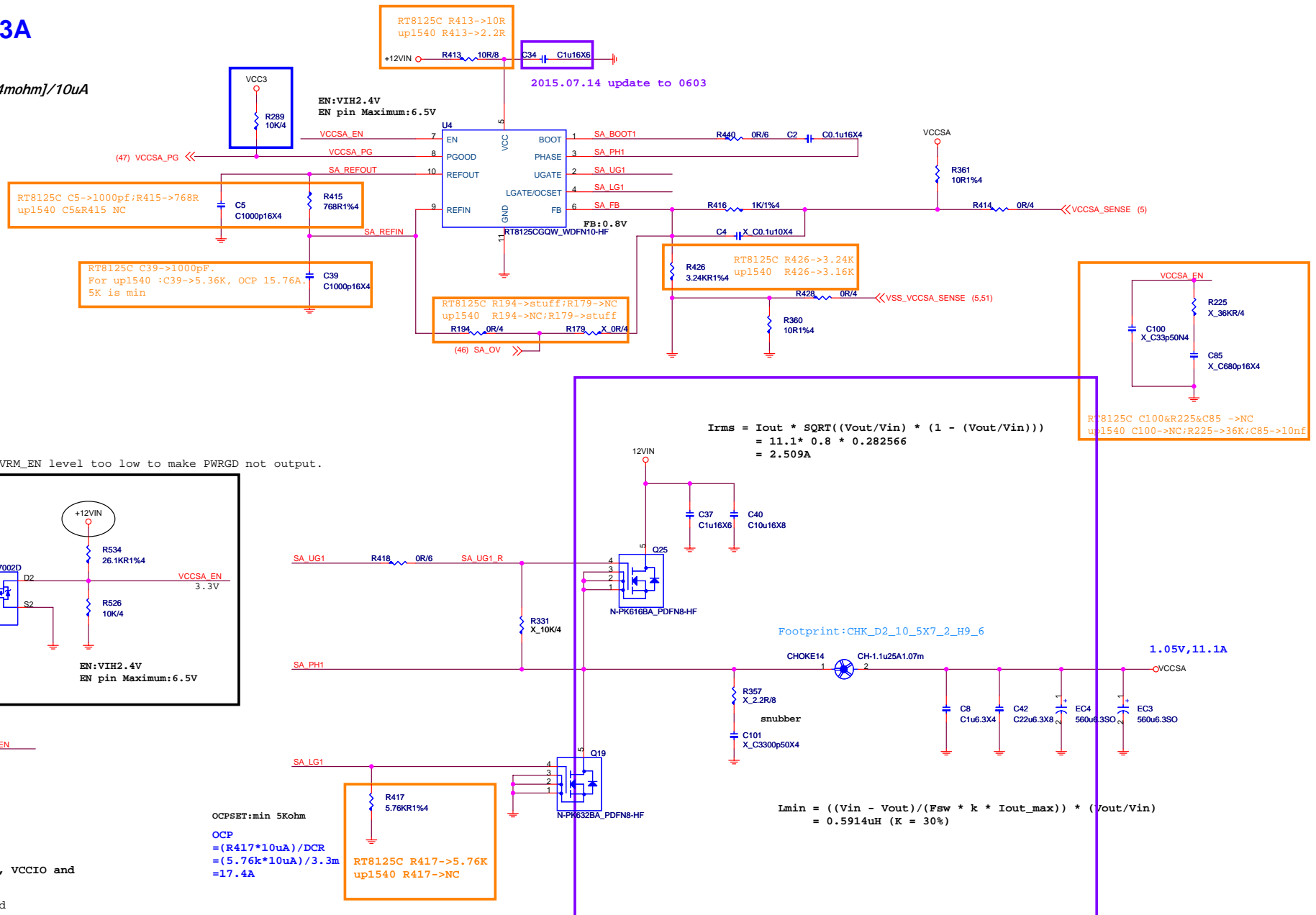
Rdson(Low)10V  
D03-4C05N03-005 : 3.4mohm  
D03-632BA0C-N03 : 3.3mohm  
D03-3056M00-U47 : 4.2mohm

2015.05.11 Update. To prevent VRM\_EN level too low to make PWRGD not output.



SLP\_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP\_S3# assertion to VR disabled  
max:1us



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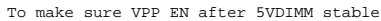
Size	Document Description	Rev
Custom	SA POWER-RT8125C-1PHASE	1.1
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Size Custom	Document Description <b>DDR POWER-RT8I25C-1PHASE</b>	Rev 1.1
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*4DIMM :2.24A FOR DDR VPP2.5V*



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MS-7970

Size Custom	Document Description <b>DDR4 Power-VPP25</b>	Rev 1.1
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# PCH\_1VSB

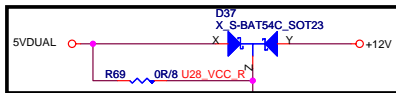
1.0V; 11A

OCP = 11.787A

Rocset =  $1.5 * I_{max} * R_{dson}(low) / I_{ocset}$   
 =  $1.5 * 7.858 * 5mohm / 10uA$   
 = 5.8935K

$R_{dson}(low) 4.5V$   
 D03-4C05N03-O05 : 5 mohm  
 D03-632BA0C-N03 : 4.6mohm  
 D03-3056M00-U47 : 6.2mohm

2015.07.14 Add +12V loading



uP1504 & RT8125  
 VCC Input Range : 4.5V to 13.2V

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5  
 L04-12A7321-L65 for Gaming 3, SLI, ECO  
 L04-12A7721-T15 for cost down

2015.05.25 Remove CUT\_VBAT to CUT\_1VSB\_EN

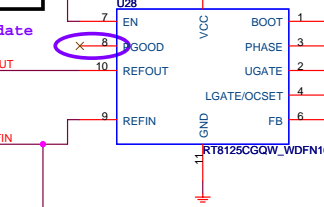


2014.08.21 update

RT8125C C236->1000pf; R204->665R  
 up1540 C236&R204 NC

RT8125C C180->1000pF.  
 For up1540 : C180->5.9K, OCP 12.82A.  
 Update 2015.05.06

2015.07.14: Change 1u/0603



RT8125C R287->stuff; R188->NC  
 up1540 R287->NC; R188->stuff

(46) PCH\_CORE\_OV

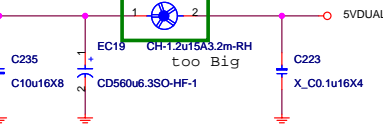
OCP  
 RT8125C R177->5.9K  
 up1540 R177->NC

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

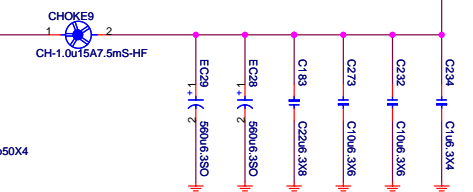
$$= 0.8 * 1.2551$$

$$= 1.004V$$



L04-01072H0-T15  
 AVL: L04-0107800-M26

MAX: 10.664A



$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in})$$

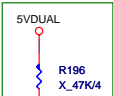
$$= 0.8335uH (K = 30\%)$$

PLACE UNDER THE PCH

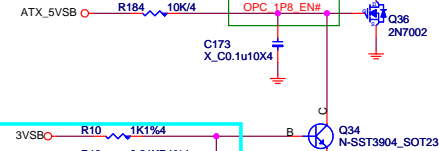
## PCH\_1P8

Remove circuit

0728: add



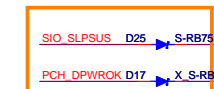
0728: Change net name



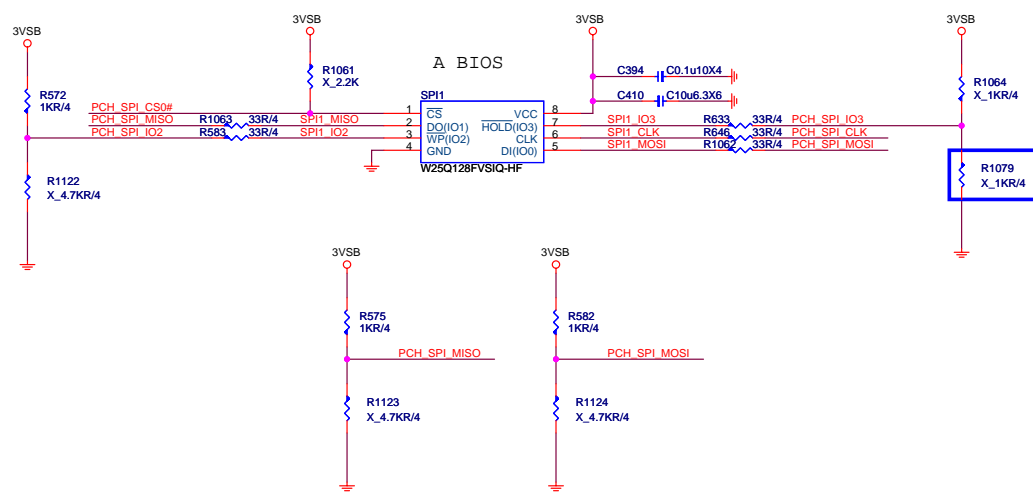
0902 : Stuff R when NO PCH\_1P8 & V\_OPC\_1P8

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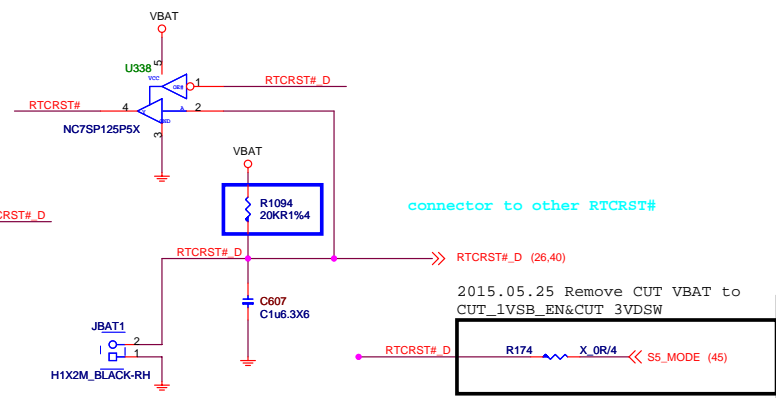
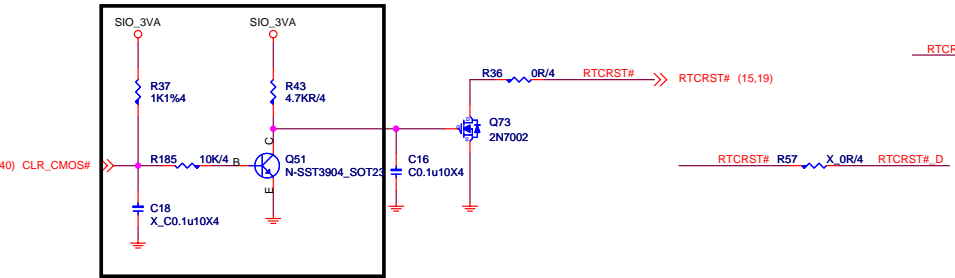
For TL624 1.1



- PCH\_SPI\_CS0# << PCH\_SPI\_CS0# (15)
- PCH\_SPI\_CLK << PCH\_SPI\_CLK (15)
- PCH\_SPI\_MISO << PCH\_SPI\_MISO (15)
- PCH\_SPI\_MOSI << PCH\_SPI\_MOSI (15)
- PCH\_SPI\_IO2 << PCH\_SPI\_IO2 (15)
- PCH\_SPI\_IO3 << PCH\_SPI\_IO3 (15)
- CHIP\_PWGD << CHIP\_PWGD (15,19,40)
- PCH\_DPWRCK << PCH\_DPWRCK (15,45)
- RSMRST# << RSMRST# (15,40)
- SIO\_SLPSUS << SIO\_SLPSUS (40,45,56)

# CLR\_CMOS

2015.04.23 Modify R37 Q51 & Add R185



2015.05.25 Remove CUT VBAT to CUT\_1VSB\_EN&CUT 3VDSW



tri-state				
INPUT			outout	
PIN1		PIN2	pin4	
L		H	H	
L		L	L	
H		X	Z	

		R57	U338	R1094	C607
USE U338	Auto CLR_CMOS	X	O	O	O
NOT USE U338	Auto CLR_CMOS	O	X	X	X

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MS-7970				
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Custom	BIOS & Clear CMOS			1.1
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## PCB



7970\_1.0

P/N:PD0-0797010-G37

## CPU Socket



## Battery



BAT-BCR2032P-RH

## PCH



D0:OB1-7968006  
D1:OB1-7982001



D0:OB1-7968004  
D1:OB1-7981001

2015.04.28 Remove LAN/Audio cover



## SBC Label



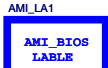
SBC LABEL

## HDMI Label



HDMI LABEL

## BIOS Label



BIOS\_LABEL

## Marketing Label



Z170-Gaming3  
MKT-LABEL



Z170-Gaming3  
X\_MKT-LABEL



Z170-Gaming3  
X\_MKT-LABEL



Z170-Gaming3  
X\_MKT-LABEL

## USB3.1 Label



U3.1 LABEL



X\_DIMM-Red



X\_PCIE-Redx16



X\_PCIE-Redx4



X\_Audio-C



X\_PS2-C



X\_USB-Black

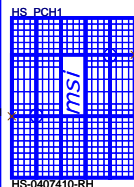


X\_LAN-Blue

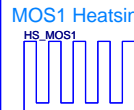


X\_USB-Blue

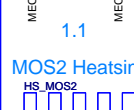
## PCH Heatsink



HS-0407410-RH



HS-0503250-RH



HS-0503250-RH



X\_PCH-HS1

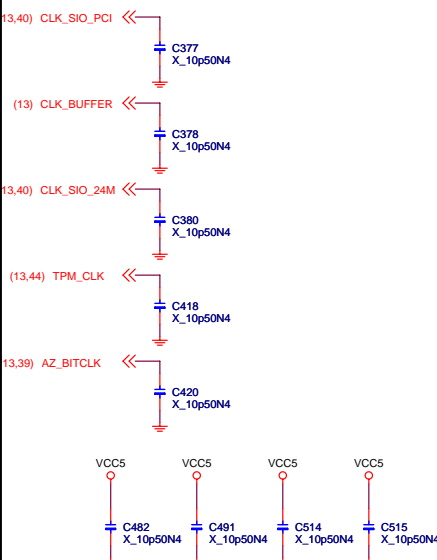


X\_MOS-HS1

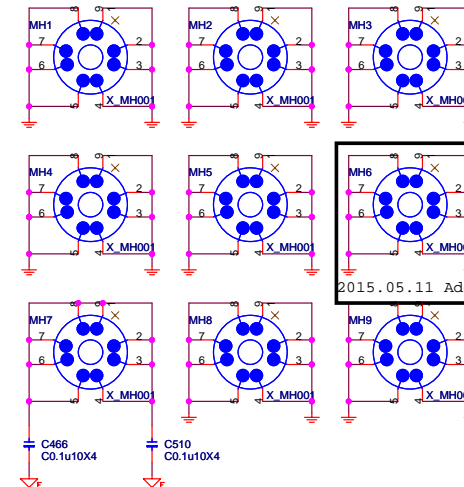


X\_MOS-HS1

2015.05.11 Add EMI suggestion



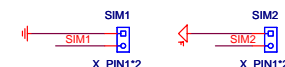
## Mounting Holes



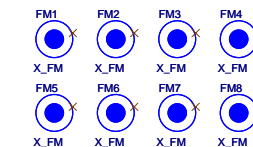
## Test point



## Simulation

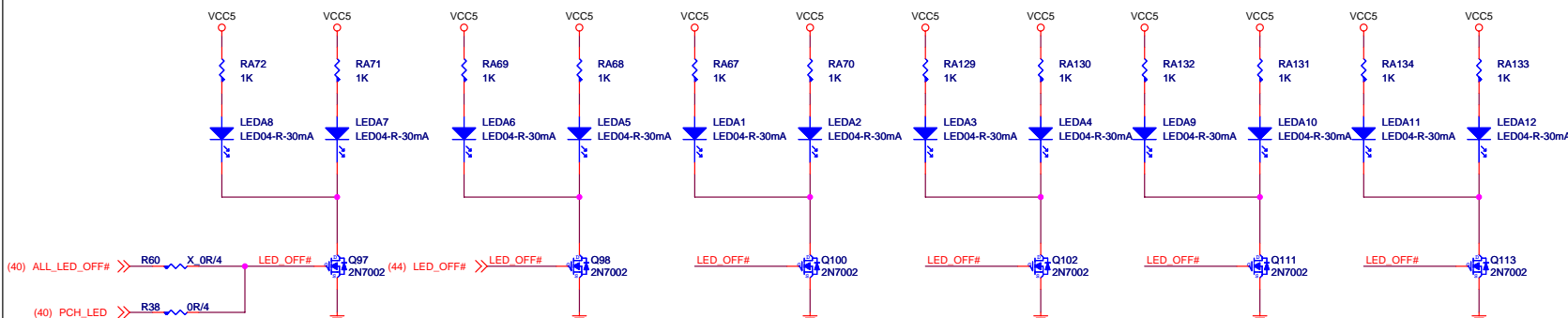


## Optical Fiducial Marks-120



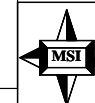
2015.04.28 Add

## LED placed in the four corners of board.



2015.07.03 Add

2015.07.03 Add




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D				D
C				C
B				B
A				A
5	4	3	2	1

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			MS-7970		
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